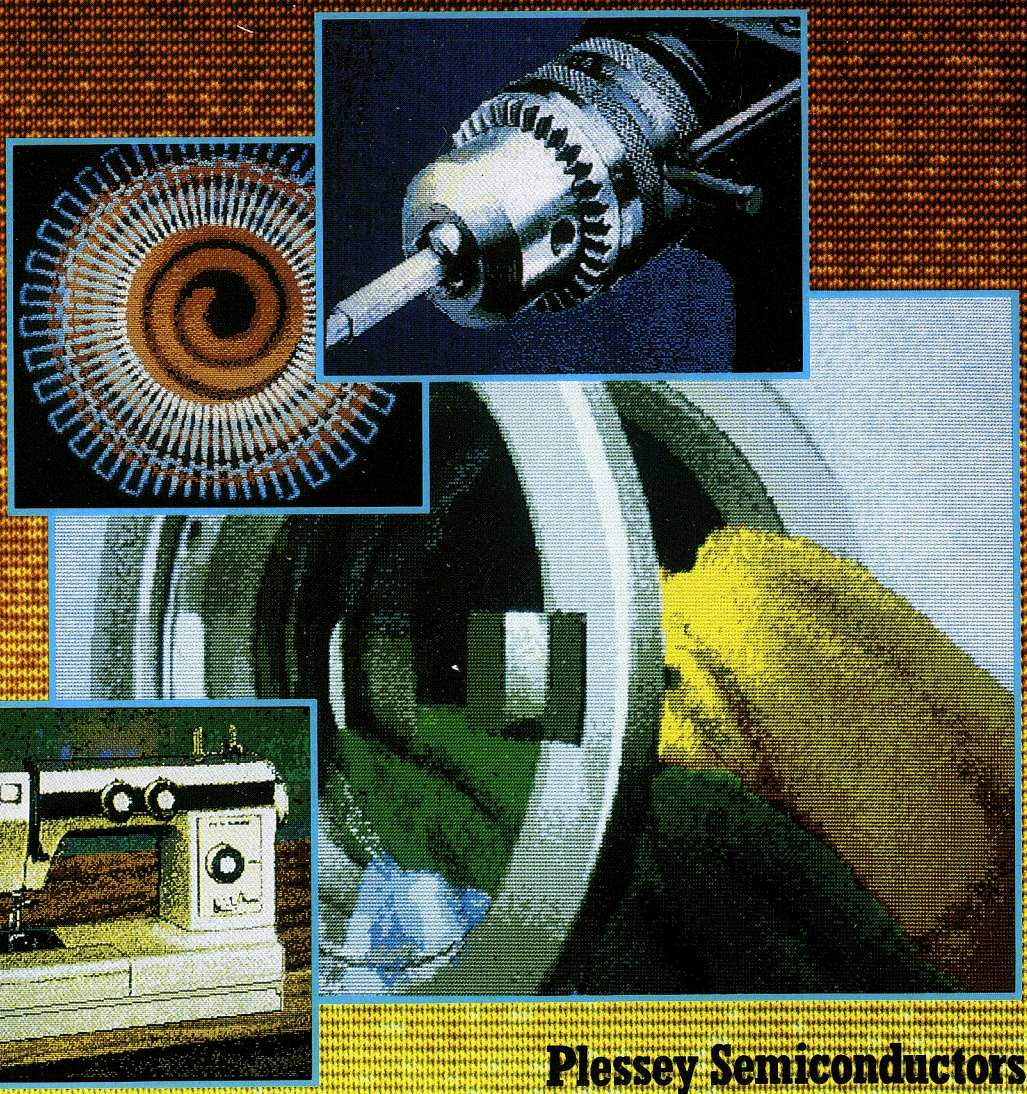
POWER CONTROL

IC Handbook



Plessey Semiconductors

POWER CONTROL
IC Handbook

PLESSEY
Semiconductors

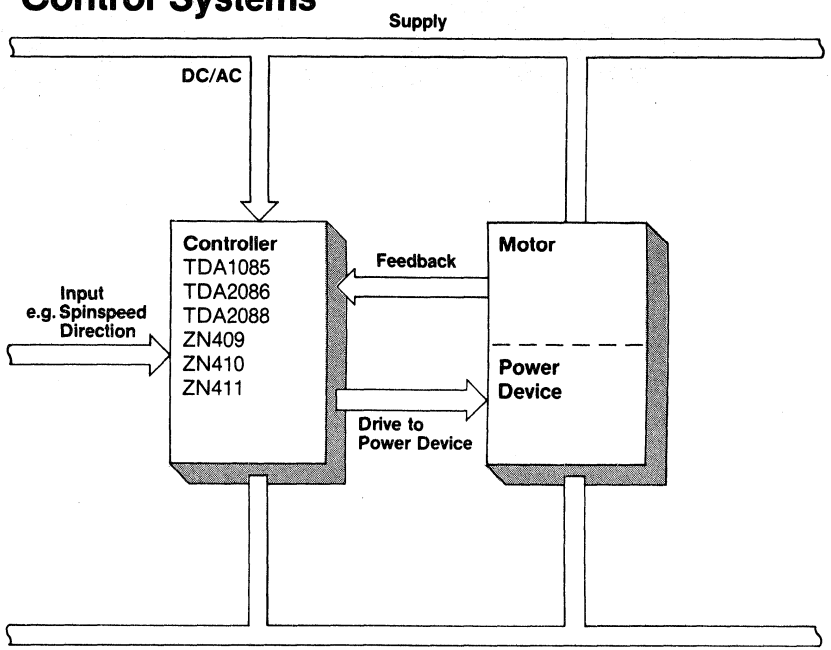
Foreword

Plessey Semiconductors range of technologies offers a versatile selection of power control circuits for consumer and industrial applications.

From radio control to washing machines; heater control to power supplies; Plessey Semiconductors expertise supports high volume, high reliability requirements.

The Quality Assurance Procedures as applied to all Plessey Semiconductors products guarantee performance and reliability in some of the harshest and noisiest environments in the consumer field: washing machines.

Motor Control Systems



Contents

	Page
Foreword	2
Product index	4
Product list - alpha numeric	5
Technical data	7
Application notes	
An electronic thermostat for room heaters using SL441C	53
SL443A application circuits	54
A design example using the SL446A	55
System design with the TDA1085C	57
System design with the TDA2086A	67
System design with the TDA2088	77
System design with the TDA2090	81
System design using the ZN409	84
System design with the ZN410	94
System design with the ZN411	101
System design with the ZN1060E	108
System design and applications for the ZN1066	114
Package outlines	131
Stop press	137
Plessey Semiconductors locations	161

Product index

Phase Controllers

Type	Function	Mains Supply	Supply Current	Output Pulse Current	Page
TDA1085C	For household appliances	50/70Hz	7.4mA	150mA	19
TDA2086	For household appliances	50/70Hz	3.1mA	125mA	24
TDA2088	Current feedback control	50/70Hz	3.1mA	125mA	29
ZN410E	Low cost universal motor speed controller	50/70Hz	3.5mA	100mA	38
ZN411	Universal motor speed controller	50/70Hz	4mA	110mA	41

Zero Voltage Switches

Type	Features	Mains Supply	Supply Current	Output Pulse Current	Page
SL441C	Proportional temperature control	50/60Hz	7.0mA	100mA min into 2V	9
SL443A	Manual power control	50/60Hz	7.2mA	80mA min into 2V	12
SL446A	Servo on/off control	50/60Hz	7.0mA	80mA min into 2V	16
TDA2090A	Proportional temp. control. 3 LED drive	50/60Hz	3.5mA	70mA into 3V	33

Precision Servo Controller

Type	Function	Supply Voltage	Supply Current	Output Drive Current	Page
ZN409CE	Precision servo controller - AC motor control	5V AC	6.7mA	50mA	36

Switching Regulators

Type	Function	Output Frequency	Supply Current	Output Current	Page
ZN1060E	Switching regulator control circuit	100kHz (max.)	12mA	40mA	44
ZN1066E/J	Switching regulator control and drive unit	500kHz (max.)	40mA	±60mA	47

Timer

Type	Function	Supply Voltage	Output Current	Page
ZN1036E/D	Programmable counter/timer	+5V	25mA	139

Product list

TYPE No.	DESCRIPTION	PAGE
SL441C	Proportional temperature control	9
SL443A	Manual power control	12
SL446A	Servo on/off control	16
TDA1085C	For household appliances	19
TDA2086	For household appliances	24
TDA2088	Current feedback control	29
TDA2090A	Proportional temperature control. 3 LED drive	33
ZN409CE	Precision servo controller -AC motor control	36
ZN410E	Low cost universal motor speed controller	38
ZN411C	Universal motor speed controller	41
ZN1060E	Switching regulator control circuit	44
ZN1066E/J	Switching regulator control and drive unit	47
STOP PRESS		
ZN1036E/D	Programmable counter/timer	139

Technical Data

PLESSEY
Semiconductors

SL441C
ZERO VOLTAGE SWITCH

The SL441C is a symmetrical burst control integrated circuit in an 8 pin DIL package. When used with a triac, AC power may be regulated by varying the number of mains cycles applied to the load in a fixed timing period. The device is especially suited to room temperature control applications including panel heaters, fan heaters etc. Zero Voltage Switching has the advantage of minimising radio frequency interference.

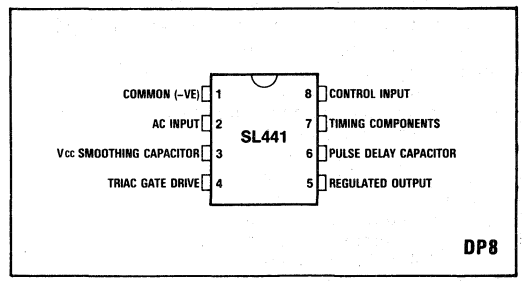


Fig.1 Pin connections (top view)

SPECIAL FEATURES

1. Balanced zero voltage point crossing detector, spike filter and pulse generator for reliable triggering of the triac.
2. A period pulse generator and bistable which are arranged to provide symmetrical burst control and eliminate $\frac{1}{2}$ wave firing. (EN50.006, BS5406, 1976)
3. A ramp generator whose output is used to modify an internal reference voltage which is then compared with the voltage appearing on the thermistor to form a proportional control system. The period of the ramp generator is defined externally and may be chosen to limit 'lamp flicker' in accordance with EN50.006/ BS5406, 1976.
4. The comparison amplifier has inbuilt hysteresis to eliminate switching jitter and a spike filter/sampling circuit to provide high immunity to both spikes and coherent 50Hz/60Hz.
5. Thermistor malfunction may be sensed and power automatically removed.
6. A supply voltage sensing circuit which inhibits firing pulses when the supply is inadequate to guarantee proper circuit operation. This eliminates stressing of the triac at switch-on.

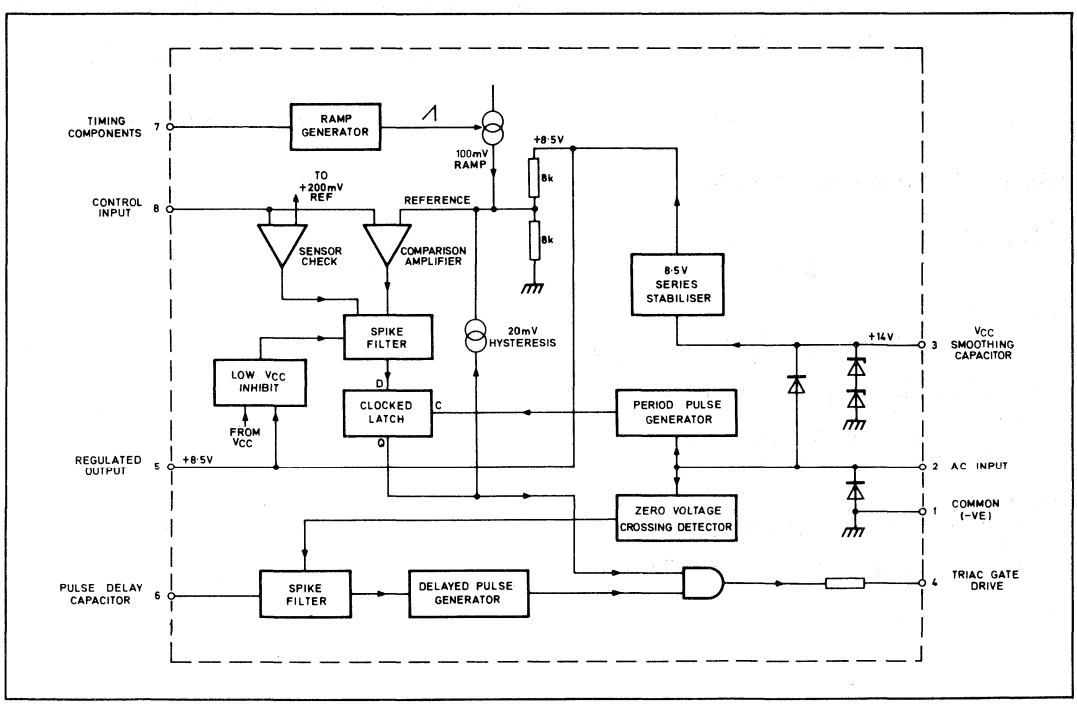


Fig.2 Block schematic of SL441C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
All voltages measured with respect to common (pin 1)

Characteristics	Value			Units
	Min.	Typ.	Max.	
Shunt regulating voltage pin 3 @ 16mA		14.7		V
Shunt regulating voltage pin 3 @ 16mA @ 75°C			16	V
Supply voltage trip level pin 3		12.2		V
Supply current (less I_4AV, I_5) (see Note 1)			7.5	mA
Regulated voltage pin 5	8.0	8.5	9.0	V
Regulated voltage temperature coefficient pin 5	−1		+1	mV/°C
Triac gate drive pin 4 (See Note 2)				
Open circuit ON voltage		8.5		V
Open circuit OFF voltage			0.1	V
Output current into 2V drain	100	130		mA
Output current into 4V drain	65	80		mA
Output current into short circuit			200	mA
Internal drain resistance		800		Ω
Control input pin 8				
Bias current			1	μA
Hysteresis		20		mV
Sensor malfunction circuit operates at	150	200	250	mV
Input working voltage range	0		12	V
Internal reference voltage (Ramp start) (See Note 3)	4.0	4.25	4.5	V
Internal reference voltage (Ramp finish) (See Note 3)		4.35		V
Peak-to-peak amplitude of ramp	70	100	130	mV
Pin 6 output impedance (R6) (See Note 2)	21.5	27	32.5	kΩ
Maximum ripple voltage pin 3			1	V_{P-P}

NOTES
1. The supply current is 0.45 x (RMS current fed into pin 2). I_5 is the current drained from pin 5 externally. I_{4AV} is the average triac gate current supplied each mains cycle.
2. Triac firing pulse. t_P Pulse width = 0.69 $R6C_D$ microseconds typical
   t_f Pulse finish = 1.09 $R6C_D$ microseconds minimum after zero voltage point R6 in kohms. C_D in nF. See Application circuit
   t_P Nominal (C_D = 2.7nF) = 50 microseconds
   t_f Minimum (C_D = 2.7nF) = 63 microseconds
3. Ramp period = 0.85 ± 0.15 x R_TC_T sec. See Application circuit. The actual value of R_T must lie between 500kohms and 3Mohms.

ABSOLUTE MAXIMUM RATINGS

Voltages
Voltage on pin 8 V_{8-1} Max. 12V
Voltage on pin 4 V_{4-1} Max. 10V

Currents
Supply current (pin 2) Peak value $\pm I_2M$ 50mA.
Non-repetitive peak current (tp $\leqslant$250μs) $\pm I_2SM$ 200mA.
Output current (pin 5) Max. 5mA Short circuit protected.
Output current (pin 4) average value $I_4(AV)$ Max 5mA Short circuit protected.

Temperature
Operating ambient temperature T_{AMB} −10°C to +75°C
Storage temperature T_{STG} −30°C to +125°C

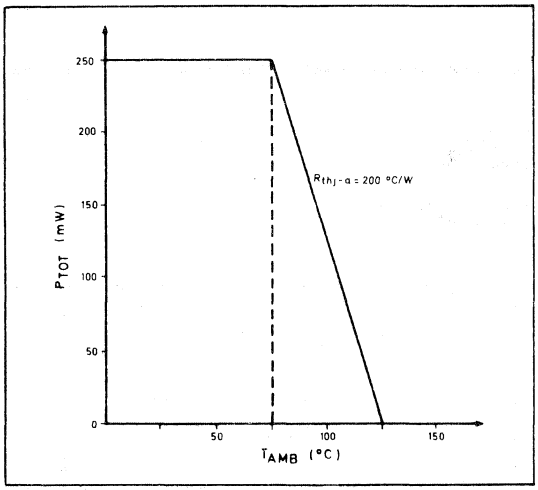


Fig. 3 Power dissipation

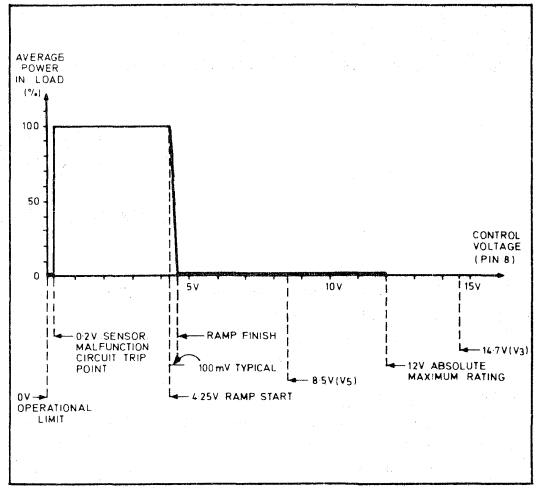


Fig. 4 Control characteristic of pin 8

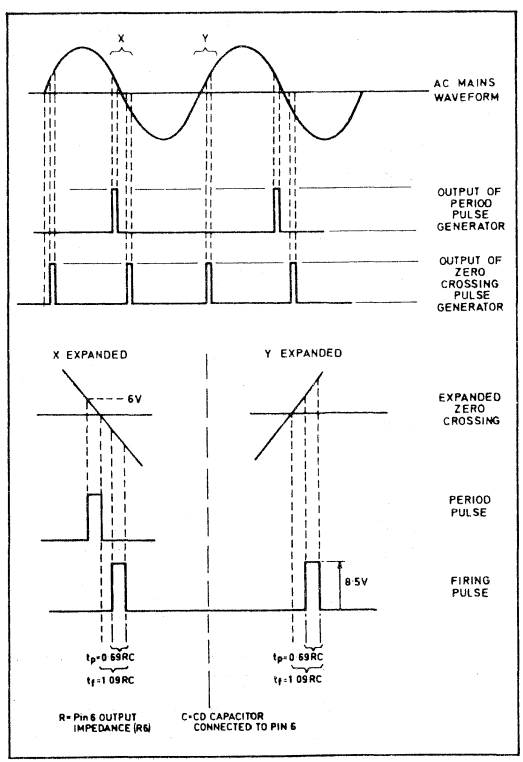


Fig. 5 Pulse timing

SL443A

ZERO VOLTAGE SWITCH

The SL443A is a symmetrical burst control integrated circuit in an 8-pin DIL plastic package and is mainly intended for manual heat control applications, for example cooker hot plates and powerful hair dryers.

SPECIAL FEATURES

1. Well defined load power/potentiometer displacement characteristics
2. High immunity against spurious triac firing under noisy mains environment (automatic spike filtration)
3. Enables compliance with Cenelec EN50,006/ BS5406-1976
   (A) Switching rate controlled
   (B) symmetrical burst control
4. Very low external component count
5. Triac firing pulses inhibited whilst the IC's power supply is being established.

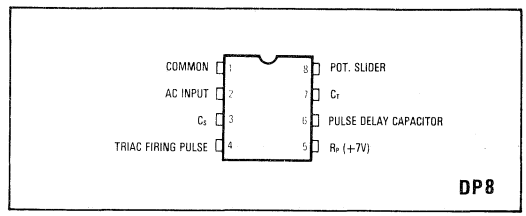


Fig.1 Pin connections - top view

APPLICATIONS

- Cooker hotplates
- Powerful hairdryers

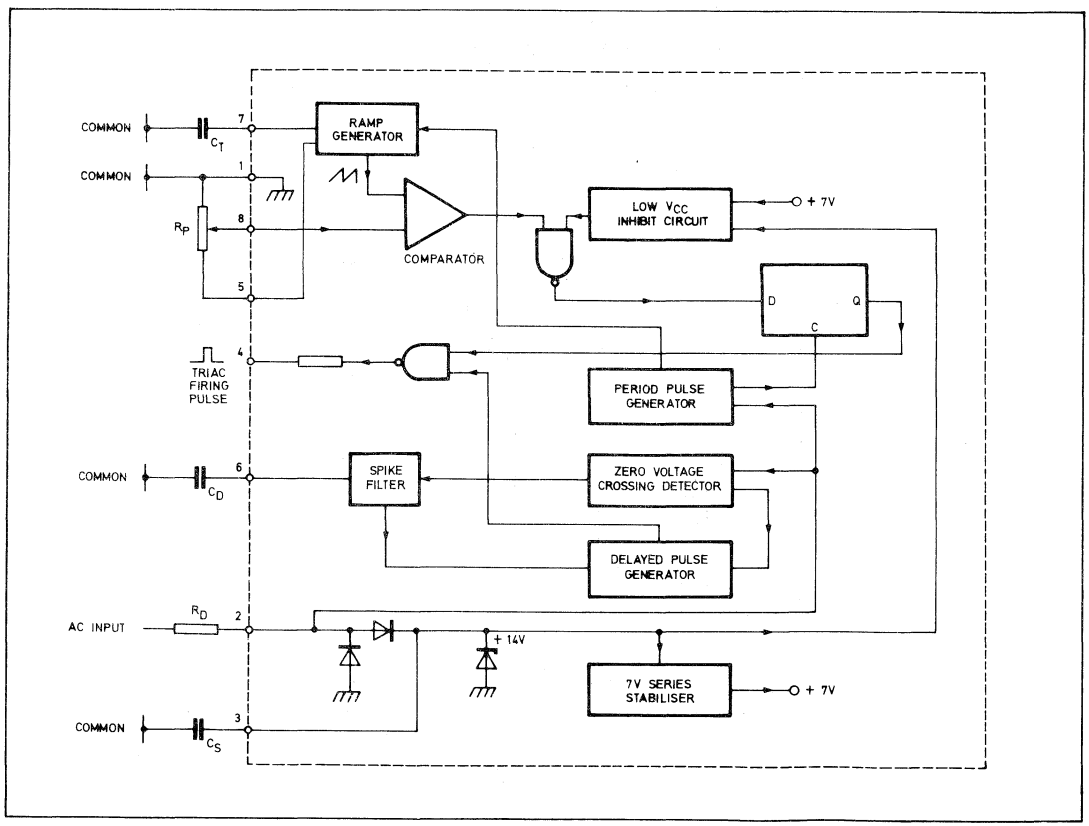


Fig.2 SL443A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C,
All voltages measured with respect to common (pin 1)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulating voltage pin 3		14.7		V	I_3 = 16mA
Shunt regulating voltage pin 3			16	V	I_3 = 16mA, T_{amb} = +75°C
Supply voltage trip level pin 3		12.2		V	
•Supply current (less I_4 AV, 2 × I_5) See Note 1			7.2	mA	
Potentiometer supply pin 5, V_5	6.8	7.0	7.6	V	
Potentiometer resistance range	18		140	kΩ	
Triac gate drive pin 4					
Open circuit ON voltage		8.5		V	
Open circuit OFF voltage			0.1	V	
Output current into 2V drain	80	100		mA	
Output current into 4V drain	50	70		mA	
Output current into short circuit			200	mA	
Internal drain resistance		800		Ω	
Control input pin 8					
Bias current			1	μA	
Internal reference – ramp start	0.3	0.5	0.7		
– ramp finish	V_5– 0.5	V_5–0.3	V_5– 0.1		
★ Period of ramp generator – T	27	30	33	s	(R_P = 100K, C_t = 0.68μ) (RMS mains voltage=220v)
Pin 6 output impedance R6	21.5	27	32.5	kΩ	

• The supply current is 0.45 x (RMS current fed into Pin 2)

★ Period of ramp = T = 2 x C_T x R_P x (RMS mains voltage) seconds

ABSOLUTE MAXIMUM RATINGS

Voltages

Voltage on pin 8,	V_{8-1}	Max	10v
Voltage on pin 4,	V_{4-1}	Max	10v

Currents

Supply current, pin 2 peak value ± I_{2M}	Max	50mA
Non-repetitive peak current ($t_P \geqslant 250\mu S$) ± I_{2SM}	Max	200mA
Output current, pin 5 I_5	Short circuit protected	
Output current, pin 4, average value I_4 (AV)	Max	10mA
	Short circuit protected	

Temperatures

Operating ambient temperature	T_{amb} —10 to 75°C
Storage temperature	T_{STG} —55 to +125°C
Power Dissipation	See Fig.3

CIRCUIT DESCRIPTION

The externally current limited AC supply is applied to the device, and rectification followed by shunt regulation provides a 14V DC supply. This is externally smoothed before application to the 7.0V series stabiliser which feeds the resistance bridge. The stabiliser must be within regulation, or operation of the 'Low Vcc Inhibit' circuit will result. This circuit overrides all other circuitry and prevents unsuitable firing pulses from being supplied to the triac at 'switch-on'. The current limited AC supply also drives the Period Pulse Generator (PPG) and zero voltage crossing circuits.

The PPG produces a single short duration pulse for each completed mains cycle and serves two purposes. Firstly it is used to clock logic information such that the circuit behaves in a symmetrical manner and only complete mains cycles are applied to the load. Secondly the pulse is used to switch timing components in the ramp generator and this enables long time constants to be achieved without having to resort to the use of electrolytic capacitors.

The zero voltage crossing detector controls a pulse generator that has a delayed output. The delay is necessary since, with loads that are slightly inductive or low power resistive, the triac load current may not reach its required holding level at zero voltage point.

Both delay and pulse duration are defined by an external capacitor and this further serves the purpose of filtering out spikes which occur in the zero crossing region. Automatic rejection takes place of spikes having a duration of up to 50 per cent of the normal width of the triac firing pulse.

The comparator amplifier has differential inputs and these are used to compare the potential appearing on the slider of the control potentiometer with that of the ramp waveform. The output of this amplifier controls the logic circuitry and the potentiometer setting defines the fraction of the ramp period for which the triac is in conduction so controlling the power in the load.

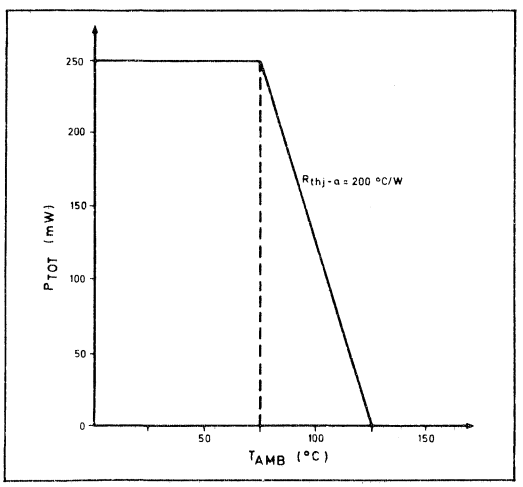


Fig. 3 Power dissipation

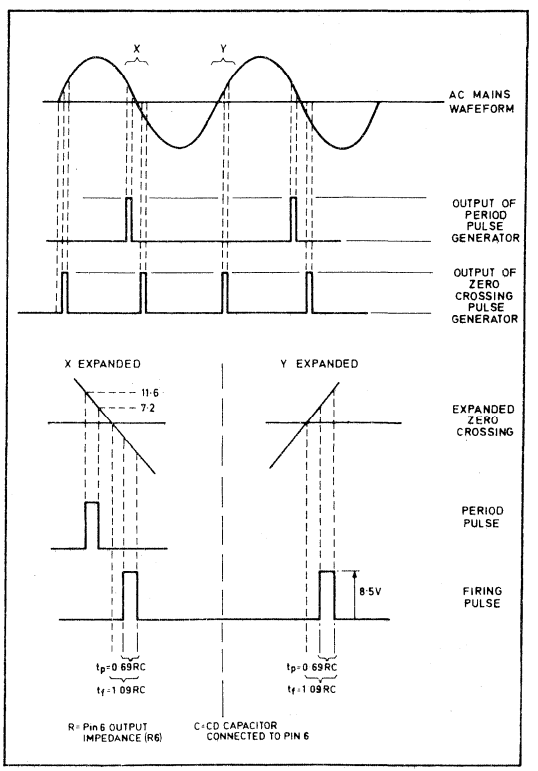


Fig.4 Pulse timing

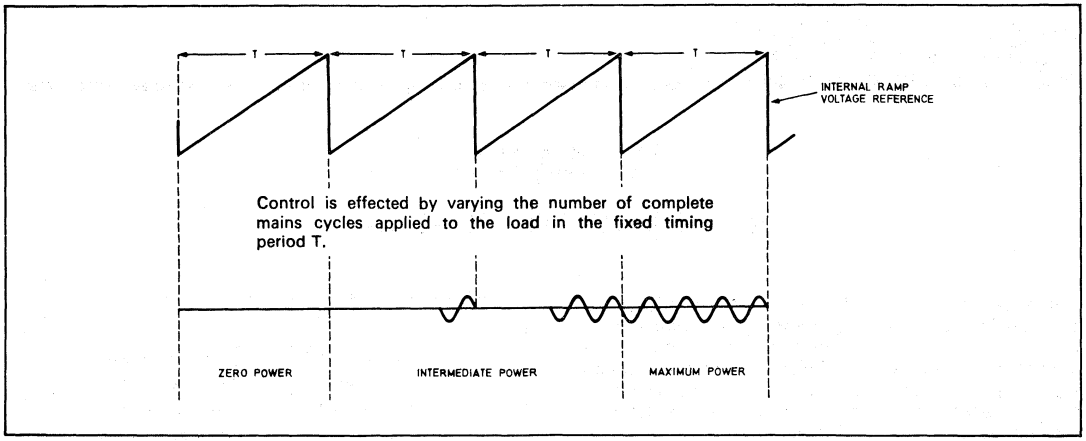


Fig. 5 Method of control

SL446A

ZERO VOLTAGE SWITCH

Intended for use in ON/OFF control of triacs, the SL446A incorporates zero voltage point triggering in order to minimise radio frequency interference. Main application areas are in switching resistive loads and replacing mechanical thermostats in, for example, central heating systems, washing machine heaters, water heaters and smoothing irons.

The SL446A is suitable for mains on-line operation and requires minimal external components.

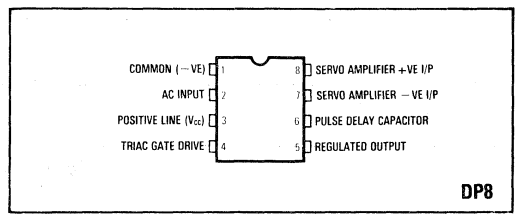


Fig.1 Pin connections - top view

FUNCTIONS

1. Balanced zero voltage point crossing detector, spike filter and pulse generator for reliable triggering of the triac.
2. A period pulse generator and bistable which are arranged to provide *symmetrical burst control* and *eliminate half-wave firing* (EN50,006/BS5406, 1976).
3. A high input impedance differential amplifier to form part of a servo system. An internally defined level of hysteresis is incorporated in the amplifier which can limit the rate of correction of the loop to meet the requirements of EN50,006/BS5406−1976, regarding flicker.
4. Internal rectification and regulation of current limited AC supply provides power for the IC and a suitable supply for the resistance bridge.
5. A supply voltage sensing circuit which inhibits firing pulses when the supply is inadequate to guarantee proper circuit operation. This effectively prevents firing pulses from being applied to the triac which are incapable of causing complete bulk conduction (possible failure mechanism at switch-on).

APPLICATIONS

- Pan Temperature Control
- Water Heaters
- Refrigerators
- Panel Heaters

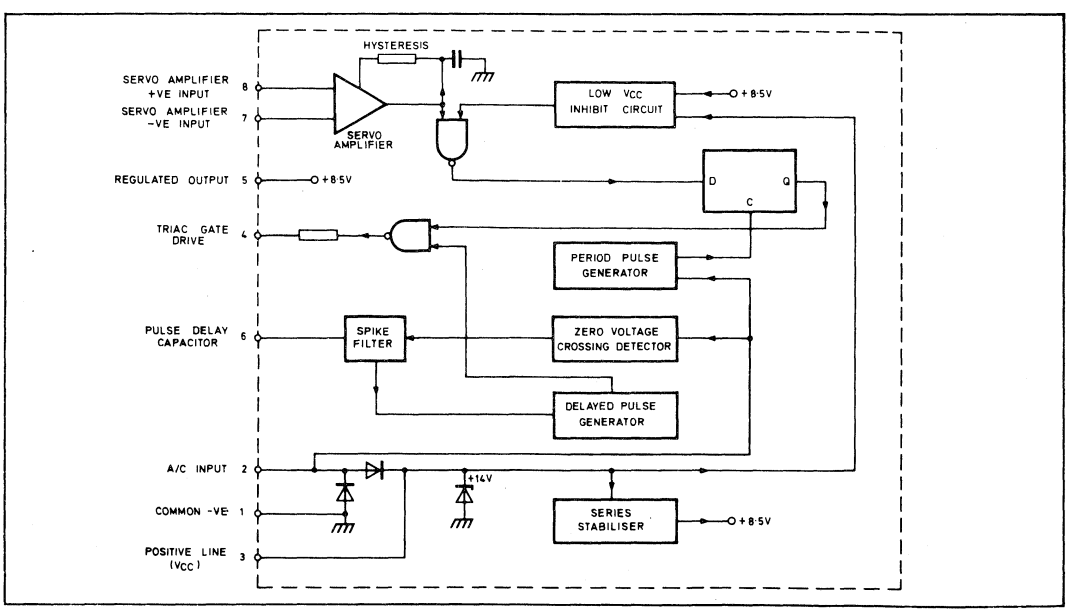


Fig.2 SL446A block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
$T_{AMB} = 25°C$,
All voltages measured with respect to common (pin 1)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulating voltage pin 3		14.7		V	$I_3 = 16mA$
Shunt regulating voltage pin 3			16	V	$I_3 = 16mA$, $T_{amb} = +75°C$
Supply voltage trip level pin 3		12.2		V	
*Supply current (less I_4 AV, I_5)			7	mA	
Regulated voltage pin 5	8.0	8.5	9.0	V	
Regulated voltage temperature coefficient pin 5	−1		+1	mV/°C	
Triac gate drive pin 4					
Open circuit ON voltage		8.5		V	
Open circuit OFF voltage			0.1	V	
Output current into 2V drain	80	100		mA	
Output current into 4V drain	50	70		mA	
Output current into short circuit			200	mA	
Internal drain resistance		800		Ω	
Servo Amplifier input bias current			2	μA	
Servo Amplifier hysteresis	20	25	35	mV	
Servo Amplifier input offset voltage	−15	0	+15	mV	
Servo Amplifier input working voltage range	0		10	V	
Pin 6 output impedance R6	21.5	27	32.5	kΩ	
Maximum ripple voltage on supply pin 3			1	Vp-p	

★ The supply current is 0.45 x (RMS current fed into Pin 2)

ABSOLUTE MAXIMUM RATINGS

Voltages
Voltage on pins 7,8 (V_{7-1} ; V_{8-1}) V_3 (14V)
Voltage on pin 4 (V_{4-1}) 10V
Currents
Supply current (pin 2):
Peak value $\pm I_{2M}$ 50mA
Non-repetitive peak current ($t_P < 250\mu s$) $\pm I_{2SM}$ 200mA
Output current (pin 5) (I_5) 10mA
Output current (pin 4), average value I_4 (AV) 10mA
Temperatures
Operating ambient temperature T_{AMB} −10°C to 75°C
Storage temperature T_{STG} −55°C to +125°C
Power dissipation See Fig.3

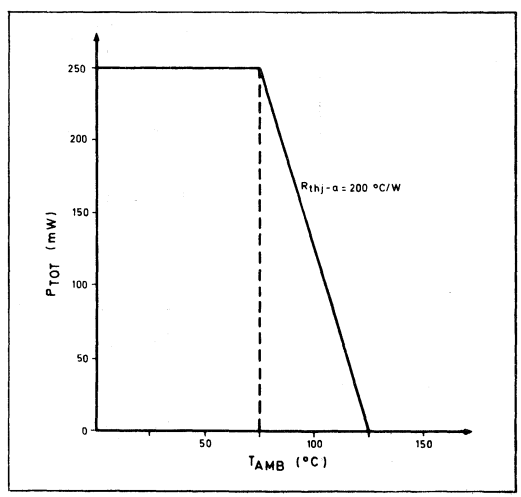


Fig.3 Power dissipation

CIRCUIT DESCRIPTION

The externally current limited AC supply is applied to the device, and rectification followed by shunt regulation provides a 14V DC supply. This is externally smoothed before application to the 8.5V series stabiliser which feeds the resistance bridge. The stabiliser must be within regulation, or operation of the 'Low Vcc Inhibit' circuit will result. This circuit overrides all other circuitry and prevents unsuitable firing pulses from being supplied to the triac at 'switch-on'. The current limited AC supply also drives the Period Pulse Generator (PPG) and zero voltage crossing circuits.

The PPG produces a single short duration pulse for each completed mains cycle. The pulse train is used to clock logic information such that the circuit behaves in a symmetrical manner and only complete mains cycles are applied to the load.

The zero voltage crossing detector controls a pulse generator that has a delayed output. The delay is necessary since, with loads that are slightly inductive or low power resistive, the triac load current may not reach its required holding level at zero voltage point.

Both delay and pulse duration are defined by an external capacitor and this further serves the purpose of filtering out spikes which occur in the zero crossing region. Automatic rejection takes place of spikes having a duration of up to 50 per cent of the normal width of the triac firing pulse.

The servo amplifier has differential inputs and these are used to sense the output of the bridge. An internally defined level of hysteresis is incorporated in the amplifier; this can limit the rate of correction of the servo loop in order to meet the requirements of EN50,006/BS5406–1976. The output of the amplifier controls the logic circuitry and the triac is triggered on at the appropriate point in the mains cycle if pin 8 is more positive than pin 7.

Triac Firing Pulse

t_p Pulse width = 0.69 R6 C_D µs typical
t_f Pulse finish = 1.09 R6 C_D µs minimum after zero voltage point. (R6 in kΩ C_D in nF – See Fig.6.)
t_p Nominal (C_D = 2.7nF) = 50µs
t_f Minimum (C_D = 2.7nF) = 63µs

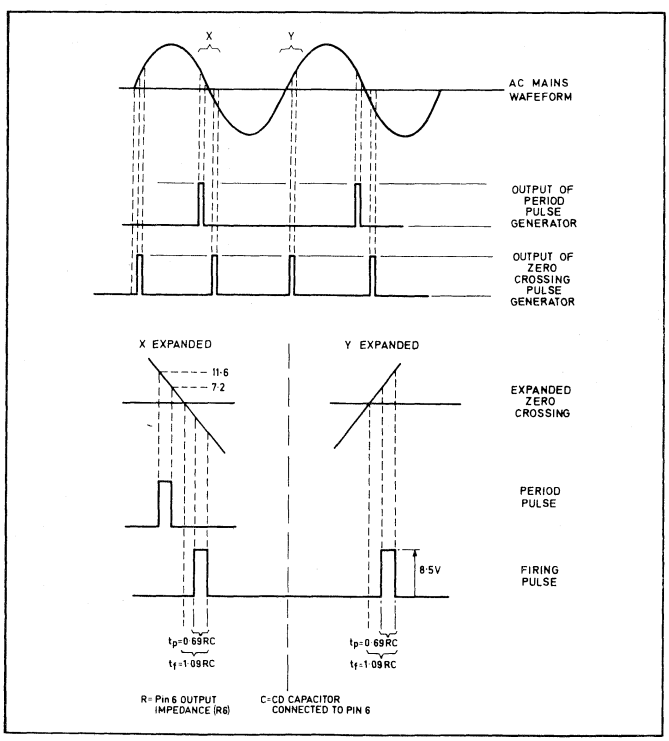


Fig. 4 Pulse timing

TDA1085C

PHASE CONTROL INTEGRATED CIRCUIT

The TDA1085C is a silicon integrated circuit designed for use in phase control systems of AC mains with resistive and inductive loads. The circuit may form the basis of closed loop control systems utilizing tacho frequency or analog voltage feedback.

The circuit was primarily designed for motor speed control in automatic washing machines and hence includes a programmable multiple ramp generator to control acceleration rates.

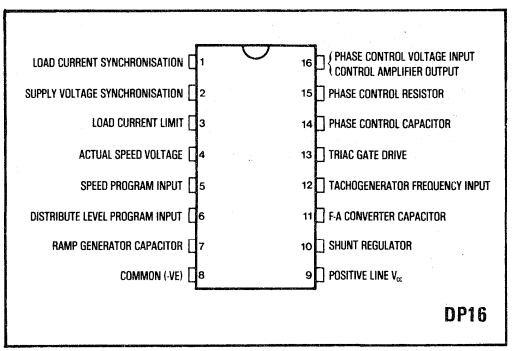


Fig.1 Pin connections - top view

SPECIAL FEATURES

- Powered direct from AC mains or DC line.
- Flexible ramp generator to provide controlled acceleration and distribution period.
- Actual speed derived from tachogenerator frequency or magnitude.
- Control amplifier allowing loop gain control.
- Symmetrical positive and negative wave firing of the triac.
- Motor current limiting.
- Fail safe in case of open circuit tachogenerator.
- Repeated triac pulses provided if triac unlatches.

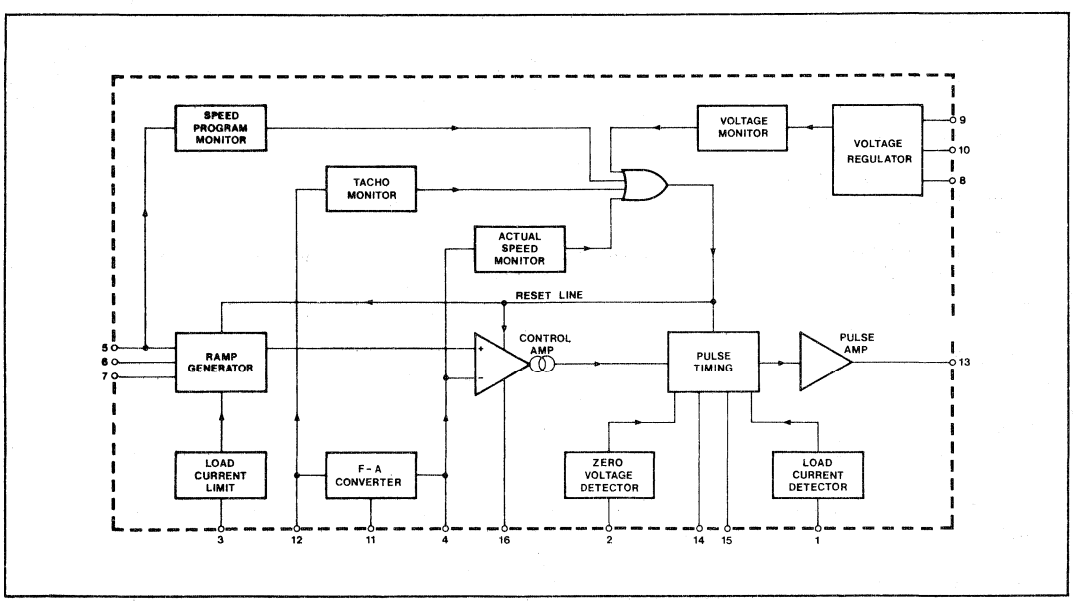


Fig.2 Block diagram of TDA1085C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$
All potentials measured with respect to common (Pin 8)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CURRENT CONSUMPTION					
Pin 9					
IC operating current		7.4	8.9	mA	Total current required is dependent on external circuitry.
VOLTAGE REGULATOR					
Pin 9					
Shunt regulating voltage		15.5	16	V	$I_9 + I_{10} = 10mA$
Monitor enable level		15.1		V	
Monitor disable level		14.5		V	
RAMP GENERATOR (See Fig.3)					
Pin 7					
Fast ramp current		1.2		mA	
Residual charging current		5		μA	During slow ramp period
Pin 5					
Speed program voltage range	0.08		13.5	V	
Bias current			-20	μA	
Pin 6					
Program distribute level	0		4	V	
Bias current			-20	μA	
Internal					
Low distribute level V_{RA}		V_6	1.2	V	Distribute levels referred to ramp generator.
High distribute level V_{RB}	$1.9V_6$	$2V_6$	$2.1V_6$	V	
FREQUENCY-ANALOG CONVERTER					
Pin 12					
Positive tacho input voltage			6	V	
Negative tacho input voltage			-3	V	
Minimum tacho input voltage	200			mV	Peak-Peak
Internal bias current		25		μA	
Pin 12 to Pin 11					
Conversion factor (typical)		7.5		mV/Hz	C pin 6 = 390pF,R pin 4 = 150kΩ
		15		mV/Hz	C pin 6 = 820pF,R pin 4 = 150kΩ
Conversion gain		10			
Linearity		±4		%	
CONTROL AMPLIFIER					
Pin 4					
Actual speed voltage limits	0		13.5	V	
Analogue input bias current			-350	nA	
Pin 4, 5 & 16					
Differential offset voltage	-60		+20	mV	$V_5 - V_4$ to give $I_{16} = 0$
Transconductance		300		μA/V	
Pin 16					
Output current drive		±100		μA	
FIRING PULSE TIMING					
Pin 2					
Voltage sync trip level		±50		μA	
Pin 1					
Current sync trip level		±50		μA	
Pin 16					
Phase control voltage swing		11.7		V	
Pin 13					
Firing pulse width		55		μs	R pin 15 = 300kΩ
Pulse repetition time		200		μs	C pin 14 = 47nF

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Pin 14					
Ramp recharge current (I_R)		150		μA	
FIRING PULSE OUTPUT DRIVE					
Pin 13					
High output level		V_{CC} - 4		V	At 150mA drive current
Leakage current			30	μA	
LOAD CURRENT LIMITER					
Pin 3 & Pin 7					
Current gain		170	—		Reset of ramp generator
Pin 7					
Discharge current		35		mA	

CIRCUIT DESCRIPTION

The TDA1085C incorporates a shunt type voltage regulator which enables it to be powered direct from the mains or from a DC supply. It can provide adequate current to drive external speed reference potential dividers that may be switched by contacts on mechanical timers. A supply monitor circuit resets timing functions and inhibits triac firing pulses when the circuit is being powered up at 'switch on'.

A ramp generator is provided to control the acceleration of the motor, to a speed as programmed on the speed program input, pin 5. If this pin becomes grounded a general reset and inhibit of triac pulses will take effect. A programmable period of slow acceleration may be used to give a 'distribution' period for automatic washing machines. Charging currents for the ramp generator are determined by an external resistor for the slow ramp period and internally during the fast ramp.

A frequency to analog (F-A) converter is provided on this device enabling advantage to be taken of tachogenerator frequency to be used for motor speed sensing. The conversion is carried out by transferring a pulse of charge (defined by the F-A converter capacitor) into an RC filter when the tacho input goes positive. An internal bias current is provided to the input pin; this serves two purposes: it senses the continuity of the tacho, causing a general reset and inhibit of output pulses if it goes open circuit; secondly it enables the input to be easily biased such that tacho noise causes no additional triggering of the F-A converter.

The control amplifier has differential inputs that compare the ramp generator voltage (internal) against the actual speed voltage. The output of this amplifier is a bidirectional current of limited amplitude which is integrated to limit the maximum rate of change of triac firing pulse phase angle. The actual speed voltage may be derived directly from a tacho (for analog sensing) or via the F-A converter circuit (for digital sensing). Digital sensing has the advantage that no tacho calibration is required, plus stability against temperature variations and ageing effects.

Synchronisation of the triac pulse is achieved by delaying the pulse with reference to the zero voltage points of the mains cycles. These points are determined by the voltage synchronisation input to the device. Inductive motors give rise to phase lag of the load current. Under high speed or heavy load conditions it is essential that the triac is fired after the load current from the previous half cycle has ceased. The current synchronisation pin (1) performs this task by ensuring that there is a voltage across the triac before a trigger pulse is supplied (when the triac is conducting current only a small voltage drop appears across it). The triac pulse width is dependent on the capacitor which also delays the pulse from the zero voltage point. If the triac fails to latch, repeated pulses will be supplied.

The current limitation pin (3) may be used to monitor the peak negative load current. This may be necessary to protect the triac and or motor under stall conditions. The trip point is determined by external resistors which when exceeded will cause the ramp generator to discharge to a safe working voltage.

RAMP GENERATOR CHARACTERISTIC

V_{RA} and V_{RB} are determined by the voltage programmed on pin 6 (V_6). Under all conditions $V_{RB} = 2V_6$, whereas $V_{RA} = V_6$ for $V_6 \leqslant 1.2V$ but is clamped at 1.2V for $V_6 \geqslant 1.2V$.

The ramp generator output voltage only rises to the desired speed voltage as defined on pin 5.

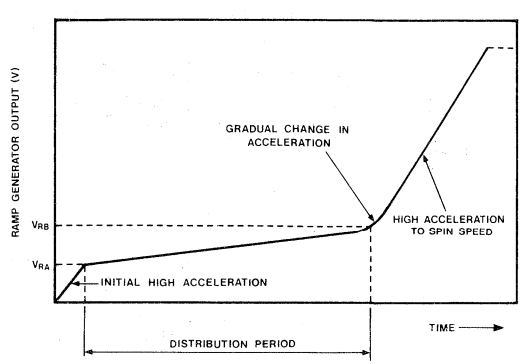


Fig.3 Ramp generator characteristic

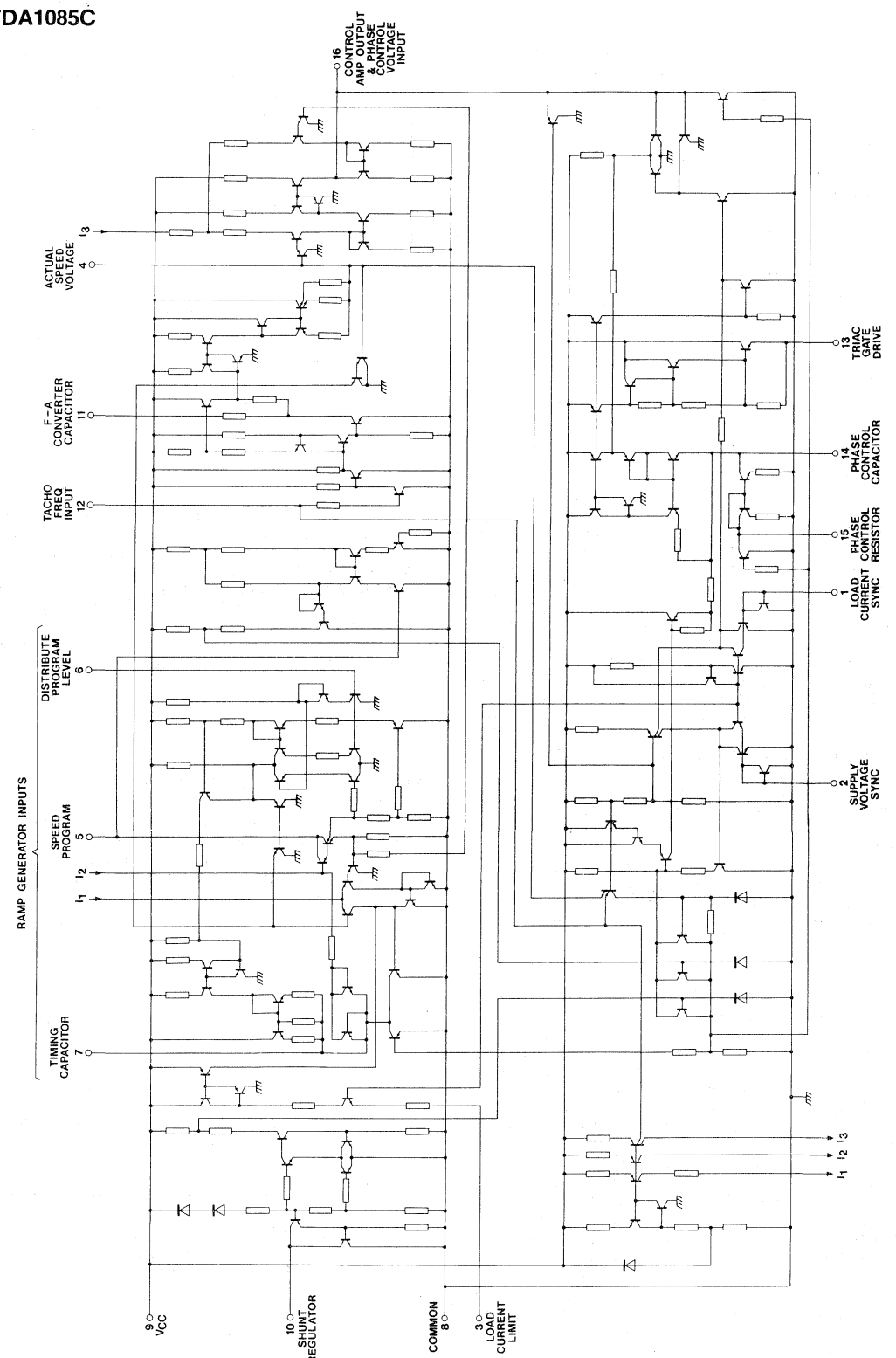


Fig.4 TDA1085C circuit diagram

ABSOLUTE MAXIMUM RATINGS

Electrical

Peak input current (I sync), pin 1:	±2mA
Peak input current (V sync), pin 2:	±2mA
Current drain, pin 3:	−5mA
Positive input voltage, pin 3:	6V
Analog voltage drive, pin 4:	V_{CC}
Speed reference voltage, pin 5:	V_{CC}
Distribute level, pin 6:	V_{CC}
IC Circuit current (pin 10 disconnected), pin 9:	10mA
Supply shunt regulating current, pin 10:	30mA
Tachogenerator (digital) drive input, pin 12:	−3, +0.1mA
Triac gate current, pin 13:	200mA
Phase timing current, pin 15:	1mA

Thermal

Operating ambient temperature:	0°C to +70°C
Storage temperature:	−55°C to +125°C

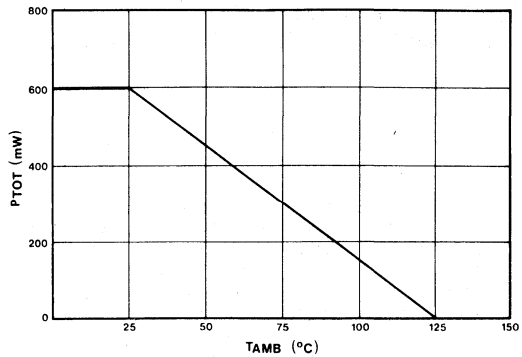


Fig.5 Power dissipation

PLESSEY
Semiconductors

TDA2086

PHASE CONTROL INTEGRATED CIRCUIT

The TDA2086 is a silicon integrated circuit designed for use in closed or open loop phase control circuits of AC with resistive or inductive loads. In closed loop systems analog voltage or tacho frequency feedback may be used.

The circuit was primarily designed for motor speed control in power drills, food mixers, washing machines etc.

In the event of an open circuit tacho generator connection the TDA2086 will demand full speed/power.

FEATURES

- Power Direct from AC Mains or DC Line
- 5V Supply Available for Ancillary Circuitry
- Low Supply Current Consumption
- Average or Peak Load Current Limiting
- Ramp Generator to Provide Controlled Acceleration
- Negative Triac Firing Pulses 100mA Guaranteed Minimum
- Warning LED Drive Circuit
- Actual Speed Derived from Tachogenerator Frequency or Analog Feedback
- Well Defined Control Voltage§Phase Angle Relationship
- Inhibit Input for use with Thermistor Temperature Sensors

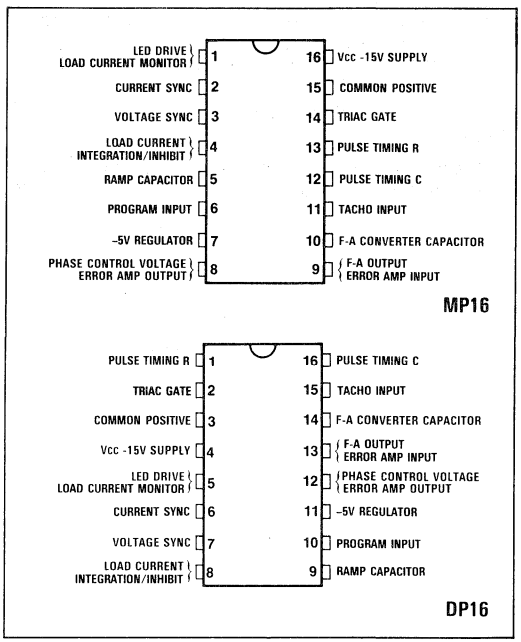


Fig.1 Pin connections - top view

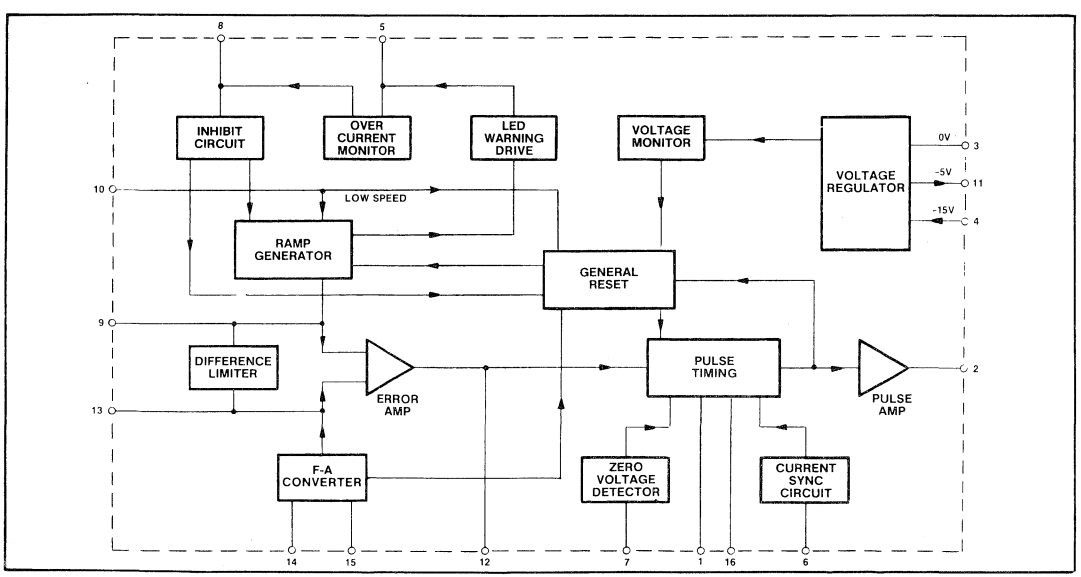


Fig.2 Block diagram of TDA2086

ELECTRICAL CHARACTERISTICS

Tests conditions (unless otherwise stated):

T_{amb} = +25° C

All potentials measured with respect to common (Pin 3) (unless otherwise stated)

Pin numbers refer to DP16 package

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CURRENT CONSUMPTION					
Pin 4					
IC Operating current		3.1	4.1	mA	Pin 4 voltage = 13.5V including triac gate drive current
SHUNT VOLTAGE REGULATOR					
Pin 4					
Regulating voltage	-16	-14.75	-13.5	V	Full temperature range
Voltage monitor enable level	-11		-9	V	
SERIES REGULATOR					
Pin 11					
Regulating voltage (Vreg)	-5.35	-5	-4.65	V	1mA external load
Temperature coefficient			±1	mV/° C	
External load			10	mA	
Regulation	-75		+75	mV	For 0-5mA external load change
RAMP GENERATOR					
Pin 9					
Capacitor charging current	25	30	35	μA	
Capacitor discharge current		25		μA	Load current limit in operation
Capacitor discharge current		10		mA	Load current inhibit in operation 5V on ramp C
Capacitor to actual speed voltage clamp	-0.8		+0.8	V	
SPEED PROGRAM CIRCUIT					
Pin 10					
Input voltage range	Vreg -0.5		0	V	
Input bias current			1	μA	
Zero power demand voltage	-100	-75	-50	mV	
FREQUENCY TO ANALOG CONVERTER					
Pin 15					
Tacho input voltage	100			mV	Peak value
Hysteresis	30	40	60	mV	
Bias current			10	μA	
Pin 15 to Pin 14					
Conversion factor (typical application)		0.5		mV/rpm	C pin 14 = 10nF, R pin 13 = 150k, 8 pole tacho 10000 rpm max.
Pin 4 to Pin 13					
Conversion gain		1			
ERROR AMPLIFIER					
Pin 9 and 13					
Input voltage range	Vreg		0	V	
Input bias current			0.5	μA	
Pin 10, 13 and 12					
Input offset voltage	-5		+15	mV	V10-V13 to give I_{12} = 0
Transconductance	80	100	120	μA/V	
Pin 12					
Output current drive	±20		±35	μA	

ELECTRICAL CHARACTERISTICS

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
FIRING PULSE TIMING					
Pin 7					
Voltage SYNC trip level	±35	±50	±65	μA	
Pin 6					
Current SYNC trip level	±35	±50	±65	μA	
Pin 12					
Phase control voltage swing	Vreg		0	V	
Pin 13					
Firing pulse width		50		μs	C pin 16 = 47nF
Pulse repetition time		100		μs	C pin 16 = 47nF, R pin 1 = 200k
FIRING PULSE OUTPUT					
Pin 2					
Drive current	100	125	150	mA	Pin 2 V = -3V
Leakage current			10μA		Pin 2 V = 0V
LOAD CURRENT LIMITING					
Pin 5					
Offset voltage			±20	mV	
Pin 5 and 8					
Current gain	0.475	0.5	0.525		Pin 5 current = 100μA
Pin 8					
Voltage for load current limit		-1V			(0.2 Vreg)
Voltage for load current inhibit		-1.5V			(0.3 Vreg)

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL	Value	Units
Triac gate voltage pin 2	4	V
Repetitive peak input current pin 4	80	mA
Non repetitive peak input current pin 4 (tp 250μs)	200	mA
Peak input current pin 5 positive half cycle	2	mA
Repetitive peak input current pin 5 negative half cycle	80	mA
Non repetitive peak input current pin 5 negative half cycle (tp 250μs)	200	mA
Peak input current (I_{SYNC}) pin 6	±1	mA
Peak input current (V_{SYNC}) pin 7	±1	mA
Inhibit input voltage pin 8	Vreg	V
-5V regulator current pin 11	10	mA
Control amp input voltage pin 13	Vreg	V
Tacho input current pin 15	±20	mA
THERMAL		
Operating ambient temperature	0 to +85	°C
Storage temperature	-55 to +125	°C

TACHO INPUT DRIVE

The TDA2086 requires less than 10μA (pk) to drive the tacho input (pin 15) and has bidirectional clamping. This makes it possible to connect a tacho pick up coil directly to the device hence minimising component count.

A motor may fail to start up if a signal is picked up by a sensitive tacho due to vibration in the rotor caused by elastic sticktion when power is initially applied. This can be easily overcome by incorporating a filtering capacitor across the tacho input.

SPECIAL FEATURES

Low Supply Current Consumption

Due to the low current consumption of the device the power dissipation in the mains dropper resistor may be as low as 1.1W on a 220V AC supply (0.5W on 110V).

By incorporating both a shunt and a series voltage regulator in the IC design, a high ripple voltage can be accommodated on the supply smoothing capacitor.

The combination of the above two features result in reduced size and a minimum count of components used in the power supply circuitry.

Powered Direct from AC Mains or DC Line

This device incorporates a shunt regulator (-15V) such that it may be powered from an AC or DC supply via current limiting components or the device may be powered direct from a -12V DC supply.

-5V Supply available for Ancillary Circuitry

A -5V series regulator is incorporated to provide a smooth supply for the internal analog control functions. This supply may be used externally to power ancillary circuitry such as timing circuits and other logic control circuits etc, as well as driving potentiometers for the analog control inputs.

Due to this supply technique, greater symmetry between positive and negative half cycle firing phase angle will result.

Low Supply Inhibit Circuit

Timing functions and triac gate drive pulses are inhibited until there is sufficient supply voltage across the device to guarantee complete gate drive pulses.

This ensures that bulk conduction is established in the triac and correct linear operation of the control system is maintained.

Negative Triac Gate Firing Pulses

Since the device works with the positive supply as common, the triac gate pulses are negative going. This is an advantage when selecting a suitable triac since most triac manufacturers prefer this drive polarity.

The device is designed to give a triac pulse that is greater than 100mA for a period of 50 microseconds with standard pulse timing components (47nF, pin 16). Repeated triac gate pulses are given if the triac fails to latch or becomes unlatched due to motor brush bounce.

Well-Defined Control Voltage/Phase Angle (Open Loop)

An internal 5V stabiliser circuit is used as the charging voltage for the pulse timing ramp capacitor and as the reference voltage for the speed input potentiometer. This ensures that maximum phase angle can be obtained by adjusting the resistor or capacitor on the pulse timing circuit, without affecting the maximum setting.

Average or Peak Load Current Limiting

The load current is normally sensed in the positive mains cycle by means of a low impedance resistor in series with the triac and load. The voltage drop across this resistor is converted back into a low current source by a second resistor and fed into the load current sensing input (pin 5) of the IC. In high load current applications where the power dissipated in a series sensing resistor would be unacceptable, a current transformer may be utilised.

The current fed into the sensing input (pin 5) is mirrored by the IC and fed to the inhibit input (pin 8). Peak current limiting can be provided at this point by inserting a resistor between pin 8 and common (pin 3), whereas average current limiting requires the addition of an integrating capacitor.

When average current limiting is used the double action of the inhibit circuit is utilised. This has two trip points such that when the first trip point (-1V) is reached the power to the load will be gradually reduced by decreasing the voltage on the ramp capacitor, (the discharge rate being equal but opposite to the soft start), hence reducing the power and providing a constant current drive (producing constant torque) to the motor. When the second trip point (-1.5V) is reached a general reset of all timing functions occurs at a fast rate, hence if a gross overload was suddenly applied to the motor, a rapid reduction in power supplied would result. Since it is not possible to turn the triac off during a cycle, the triac and motor should be chosen to be capable of withstanding one complete mains cycle under the worst overload condition.

Peak load current limiting tends to produce a fold back action (of motor speed and torque) at large conduction phase angle. This is due to the peak current initially increasing when the phase conduction angle is reduced at constant load torque.

Ramp Generator to provide Controlled Acceleration

The ramp generator is a follower integrator design which can be used to control the acceleration rate up to the programmed speed. This can also be used to control the rate of phase angle increase in open loop control systems.

The ramp rate is defined by an internal current source (25 microamps) and the capacitor connected to pin 9.

Warning LED Drive Circuit

The LED drive circuit is designed to drive an LED in series with the device such that the overall current consumption is minimised by utilising the IC drive current to power the LED. Due to the multiplexing technique on pin 5, some additional current will be required when the circuit is used to provide both load current limit and LED drive (this will normally be about 0.5mA).

The LED will illuminate under one of the following two conditions:

1. The programme speed (or phase in open loop systems) is set for zero.
2. The running speed is less than that programmed.

Hence, indication will be given when the system is powered up but zero power demanded, or when the machine cannot maintain the set operating speed due to the load current circuit operating. The LED will also be illuminated while the soft start function is in operation i.e., the LED will turn off only when the set speed has been reached.

Actual Speed Derived from Tacho Generator Frequency or Analog Feedback

Tacho frequency or analog feedback may be used with this device. When frequency feedback is used, the frequency to analog (F-A) conversion circuit is used. This circuit is extremely linear and tracks the regulated (-5V) supply.

Frequency feedback has the advantage of not being dependent on mechanical clearance, magnetic strength, etc., and since the conversion rate is defined by two external components, accurate speed programming can be obtained without the need for calibration.

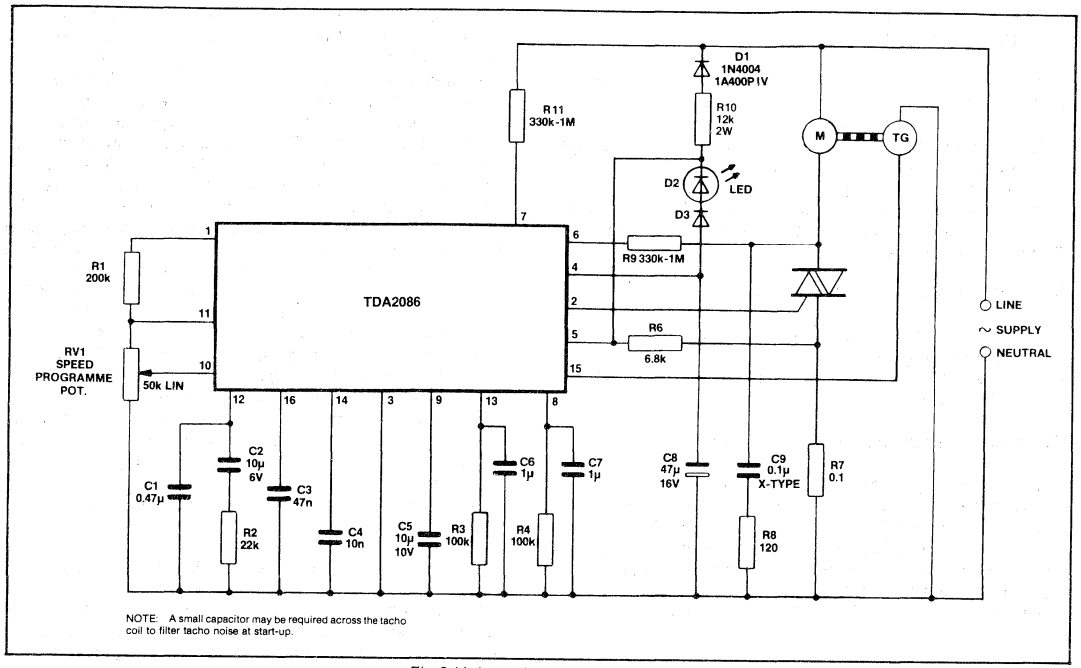


Fig.3 Universal motor application

PLESSEY
Semiconductors

TDA2088

PHASE CONTROL INTEGRATED CIRCUIT FOR CURRENT FEEDBACK APPLICATIONS

The TDA2088 is a bipolar integrated circuit phase controller, optimised for use in current feedback applications. It can also be used in open loop mode. The circuit was primarily designed for motor speed control in applications such as power tools and domestic appliances (foodmixers etc.).

FEATURES

- Powered Direct from AC Mains or DC Line
- -5V Supply Available for Ancillary Circuitry
- Low Supply Current Consumption
- Negative Triac Firing Pulses
- Guaranteed Minimum 100mA Triac Drive Current
- Well-Defined Control Voltage/Phase Angle Relationship
- Speed Compensated by Sensing Motor Current
- Simple Optimisation of Control Loop Parameters

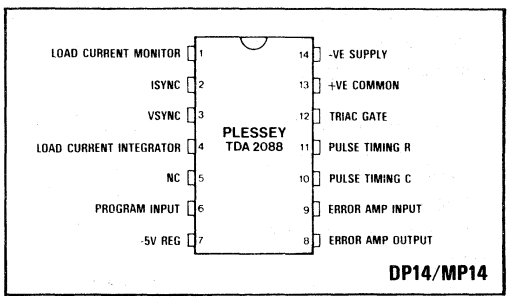


Fig.1 Pin connections - top view

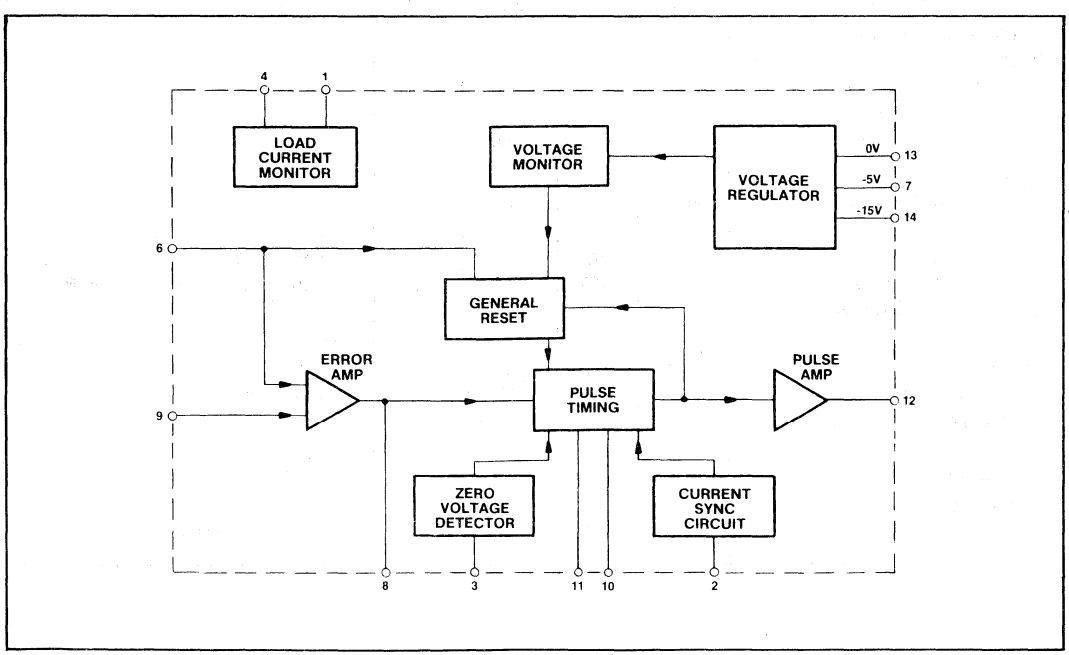


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25° C

All potentials measured with respect to common (Pin 13) (unless otherwise stated)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CURRENT CONSUMPTION					
Pin 14					
IC operating current		2.8	3.8	mA	Includes triac gate current for 50μs pulse
SHUNT VOLTAGE REGULATOR					
Pin 14					
Regulating voltage	-16	-14.75	-13.5	V	Full temperature range
Voltage monitor enable level	-11		-9	V	
SERIES REGULATOR					
Pin 7					
Regulating voltage (Vreg)	-5.35	-5	-4.65	V	1mA external load
Temperature coefficient			±1	mV/° C	
External load			10	mA	
Regulation	-75		+75	mV	For 0-5mA external load change
SPEED PROGRAM INPUT					
Pin 6					
Input voltage range	Vreg -0.5		0	V	
Input bias current			1	μA	
Zero power demand voltage	-100	-75	-50	mV	
ERROR AMPLIFIER					
Pin 6, 8 and 9					
Input offset voltage	-5		+15	mV	$V_6 - V_9$ to give $I_8 = 0$
Transconductance	80	100	120	μA/V	
Pin 8					
Output current drive	±20		±35	μA	
FIRING PULSE TIMING					
Pin 3					
Voltage SYNC trip level	±35	±50	±65	μA	
Pin 2					
Current SYNC trip level	±35	±50	±65	μA	
Pin 8					
Phase control voltage swing	Vreg		0	V	
Pin 10					
Firing pulse width		50		μs	C pin 10 = 47nF
Pulse repetition time		100		μs	C pin 10 = 47nF, R pin 11 = 200k
FIRING PULSE OUTPUT					
Pin 12					
Drive current	100	125	150	mA	Pin 12 V = -3V
Leakage current			10	μA	Pin 12 V = 0V
LOAD CURRENT SENSING					
Pin 1					
Offset voltage			±20	mV	
Pin 1 and 4					
Current gain	0.475	0.5	0.525		Pin 1 current = 100μA

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL	Value	Units
Triac gate voltage pin 12	4	V
Repetitive peak input current pin 14	80	mA
Non repetitive peak input current pin 14 (tp = 250μs)	200	mA
Non repetitive peak input current pin 1 negative half cycle (tp 250μs)	200	mA
Peak input current (I_{SYNC}) pin 2	±1	mA
Peak input current (V_{SYNC}) pin 3	±1	mA
-5V regulator current pin 7	10	mA
Control amp input voltage pin 9	Vreg	V
THERMAL		
Operating ambient temperature	0 to +85	°C
Storage temperature	-55 to +125	°C

SPECIAL FEATURES

Low Supply Current Consumption

Due to the low current consumption of the device the power dissipation in the mains dropper resistor may be as low as 1.1W on a 220V AC supply (0.5W on 110V).

By incorporating both a shunt and a series voltage regulator in the IC design, a high ripple voltage can be accommodated on the supply smoothing capacitor.

The combination of the above two features result in reduced size and a minimum count of components used in the power supply circuitry.

Powered Direct from AC Mains or DC Line

This device incorporates a shunt regulator (-15V) such that it may be powered from an AC or DC supply via current limiting components or the device may be powered direct from a -12V DC supply.

-5V Supply available for Ancillary Circuitry

A -5V series regulator is incorporated to provide a smooth supply for the internal analog control functions. This supply may be used externally to power ancillary circuitry such as timing circuits and other logic control circuits etc, as well as driving potentiometers for the analog control inputs.

Due to this supply technique, greater symmetry between positive and negative half cycle firing phase angle will result.

Low Supply Inhibit Circuit

Timing functions and triac gate drive pulses are inhibited until there is sufficient supply voltage across the device to guarantee complete gate drive pulses.

This ensures that bulk conduction is established in the triac and correct linear operation of the control system is maintained.

Negative Triac Gate Firing Pulses

Since the device works with the positive supply common, the triac gate pulses are negative going. This is an advantage when selecting a suitable triac since most triac manufacturers prefer this drive polarity.

The device is designed to give a triac pulse that is greater than 100mA for a period of 50 microseconds with standard pulse timing components (47nF, pin 10). Repeated triac gate pulses are given if the triac fails to latch or becomes unlatched due to motor brush bounce.

Well-Defined Control Voltage/Phase Angle Relationship

An internal -5V reference circuit is used as the charging voltage for the pulse timing ramp capacitor and as the reference voltage for the speed input potentiometer. This ensures that maximum phase angle can be obtained by adjusting the resistor or capacitor on the pulse timing circuit, without affecting the maximum setting.

Average Load Current Sensing

The load current is normally sensed in the positive mains half-cycle by means of a low impedance resistor in series with the triac and load. The voltage drop across this resistor is converted back into a low current source by a second resistor and fed into the load current sensing input (pin 1) of the IC. In high load current applications where the power dissipated in a series sensing resistor would be unacceptable, a current transformer may be utilised.

PLESSEY
Semiconductors

TDA2090A

ZERO VOLTAGE SWITCH

The TDA2090 is a symmetrical burst control zero voltage switch designed for temperature control in smoothing irons, water heaters, refrigerators, room heaters etc.

The circuit is designed to eliminate half wave firing and has a programmable switching rate to eliminate lamp flicker (EN50.006, BS5406, 1976).

FEATURES

- 3 LED Drive Circuit Indicates High, Low or In-band for Controlled Temperature
- Symmetrical Negative Triac Firing Pulses about the Mains Zero Voltage Points to Minimise RFI
- Programmable Switching Rate, Proportional Band and LED Indicator Window
- -5V Supply for Sensing, Thermistor Bridge and Ancillary Control Circuits
- Open Circuit Sensor Thermistor Detector demands Zero Power and Lights Over-temperature LED
- Powered Direct from Mains via Current Limiting Components or from DC Line

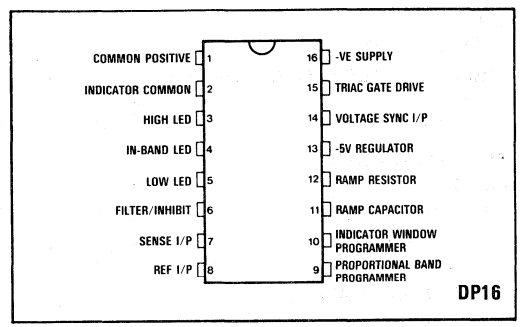


Fig.1 Pin connections - top view

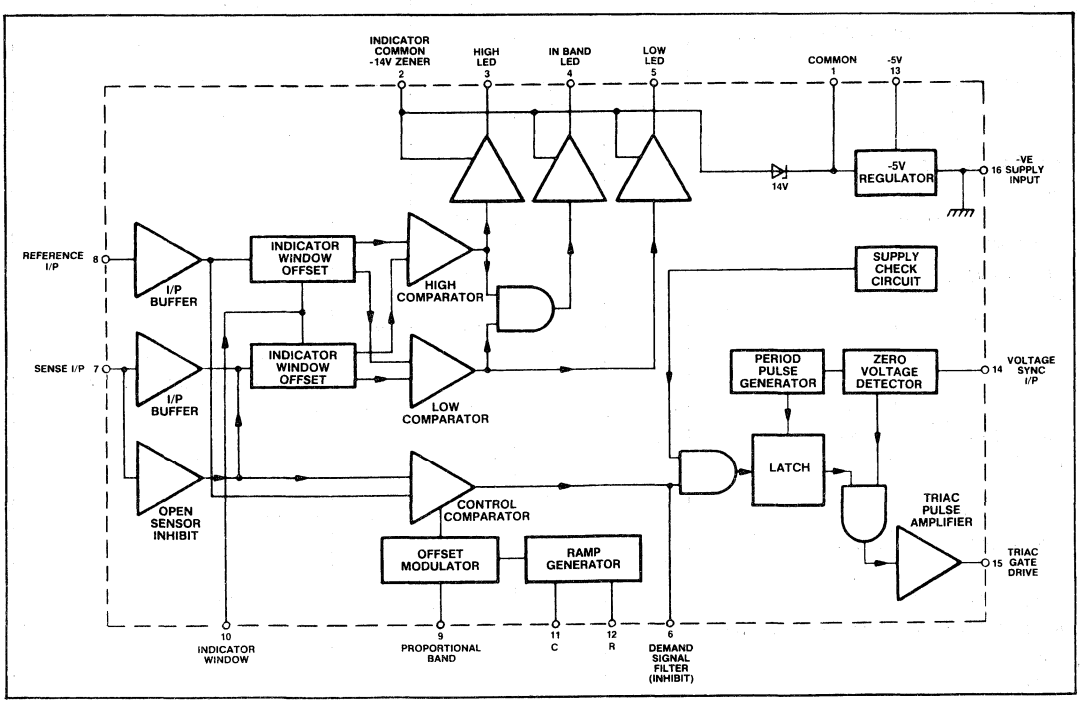


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CURRENT CONSUMPTION					
Pin 16					
IC operating current		3.5	5.5	mA	Not including triac gate or bridge supply current
VOLTAGE MONITOR					
Pin 16					
Voltage monitor enable level	-11		-9	V	
SHUNT VOLTAGE REGULATOR (V_{EE})					
Pin 2					
Regulating voltage	-13.5	-13.5	-15.5	V	
SERIES REGULATOR					
Pin 13					
Regulating voltage (V_{reg})	-5.35	-5	-4.65	V	1mA external load
External current			5	mA	
Regulation	120		120	mV	For 0-5mA load change
CONTROL COMPARATOR					
Pins 6,7,8					
Proportional control band	±20	±50	±80	mV	Pin 9 = -0.5
Proportional control band	±140	±200	±260	mV	Pin 9 = -2V
Pins 7,8					
Input bias current			2	μA	
Hysteresis		10		mV	
Pin 7					
OPEN SENSOR inhibit level	20		40	mV	With respect to V_{reg}
INDICATOR WINDOW COMPARATORS					
Pins 7,8					
Indicator window	±50	±100	±150	mV	Pin 10 = -0.5V
Indicator window	±300	±400	±500	mV	Pin 10 = -2V
Indicator window hysteresis	10		30	mV	
FILTER/INHIBIT INPUT					
Pin 6					
Output drive current	±10		±50	μA	
Inhibit trip level	-3.5		-2.6	V	
LED DRIVE CIRCUIT					
Pins 3,4,5					
LED drive current			40	mA	
High output voltage		6.4		V	Output current = 20mA Pin 2 connected to common
Output leakage current			10	μA	Output voltage = V_{EE}
TRIAC PULSE AMPLIFIER					
Pin 15					
Drive current	50	75	95	mA	Pin 15 = -3V
Leakage current			10	μA	Pin 15 = 0V
WINDOW PROGRAMMER					
Pin 10					
Input bias current			2	μA	Pin 10 = 0V
PROPORTIONAL BAND PROGRAMMER					
Pin 9					
Input bias current			2	μA	Pin 9 = 0V

ELECTRICAL CHARACTERISTICS (Continued)

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
RAMP GENERATOR					
Pin 11					
Ramp Capacitor charge current	-12		-6	μA	With 470k resistor from
Ramp capacitor discharge current	6		12	μA	Pin 12 to 0V
Upper ramp trip voltage	-1.0		-2.5	V	
Lower ramp trip voltage	-6.5		-5.5	V	
Pin 12					
Ramp programming current	5		50	μA	
VOLTAGE SYNCHRONISATION					
Pin 14					
Voltage synchronisation trip level (I_{sync})	±20	±25	±30	μA	
Period pulse trip level	35	50	75	μA	

ABSOLUTE MAXIMUM RATINGS

	Value	Units
ELECTRICAL		
-14V shunt regulator repetitive peak input current pin 2	100	mA
Non repetitive peak input current pin 2 ($t_p < 250\mu s$)	250	mA
Repetitive peak input current pins 3,4,5	100	mA
Non repetitive peak input current pins 3,4,5 ($t_p < 250\mu s$)	250	mA
Peak input current pin 14	±5	mA
-5V regulator current pin 13	10	mA
Supply voltage pin 16	-18	V
Voltage on pins 6,7,8,9,10	V_{reg}	V
Triac gate voltage pin 15	4	V
Ramp current pin 12	0.5	mA
THERMAL		
Operating ambient temperature	0 to 60	°C
Storage temperature	-55 to +125	°C

CIRCUIT DESCRIPTION

Power is supplied direct from the mains via current limiting components to a nominal 14V zener. An external capacitor maintains a smooth DC supply between mains cycles. The -14V supply is monitored by the supply check circuit which prevents unsuitable firing pulses being applied to the triac if the supply is less than that required to guarantee correct circuit operation.

A separate -5V series stabiliser provides internal biasing and a smooth external supply for the thermistor bridge and any ancillary control circuitry.

A differential input comparator compares the measured temperature with the set temperature to determine whether a power demand condition exists. A programmable triangular wave oscillator and modulator can vary the comparator offset such that a proportional control band and controlled switching rate are provided. Filtered and latched hysteresis feedback prevents switching jitter due to interference.

The power demand signal from the comparator is clocked into the latch by the period pulse which occurs once in each mains cycle, thus preventing halfwave firing of the triac.

The zero voltage detector generates a symmetrical pulse about the zero voltage points of the mains cycle. When gated by the latch output and amplified by the triac pulse amplifier the pulse provides the negative triac gate drive. By sensing the current in the voltage sync. pin (14) symmetrically about the zero voltage point, a firing pulse is produced which will maintain the triac in conduction throughout the entire mains cycle, thus minimising RFI. The width of the firing pulse is set by the external resistor in series with pin 14.

The device is capable of driving 3 LEDs to indicate a high, low or in-band temperature condition. The LEDs are connected in series with the device to reduce current consumption when power is provided direct from the mains via current limiting components, or in parallel when a DC supply is used.

The indicator window which determines the range of temperature over which the in-band LED is on, is programmed by the voltage applied to the indicator window programming pin (10). A similar input sets the width of proportional band for the control comparator. To minimise external component count, the indicator window and proportional band programming inputs (pins 10 and 9) may be connected to the same external voltage. Under these conditions the indicator window is twice the proportional control band.

ZN409CE

PRECISION SERVO INTEGRATED CIRCUIT

The ZN409CE is a precision monolithic integrated circuit designed particularly for pulse-width position servo mechanisms used in all types of control applications. The low number of components required with the ZN409CE, together with its low power consumption, make this integrated circuit ideal for use in model aircraft, boats and cars where space, weight and battery life are at a premium. The amplifier will operate over a wide range of repetition rates and pulse widths and is therefore suitable for the majority of systems. The ZN409CE can also be used in motor speed control circuits.

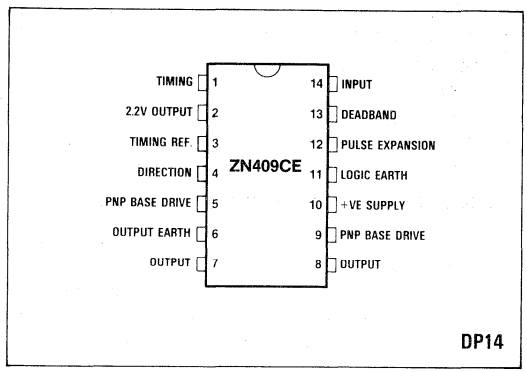


Fig.1 Pin connections - top view

FEATURES

- Low External Component Count
- Low Quiescent Current (7mA Typical at 4.8V)
- Excellent Voltage and Temperature Stability
- High Output Drive Capability
- Consistent and Repeatable Performance
- Precision Internal Voltage Stabilisation
- Time Shared Error Pulse Expansion
- Balanced Deadband Control
- Schmitt Trigger Input Shaping
- Reversing Relay Output (DC Motor Speed Control)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.5V
Package dissipation	300mW
Operating temperature range	-20 °C to +65 °C
Storage temperature range	-65 °C to +150 °C

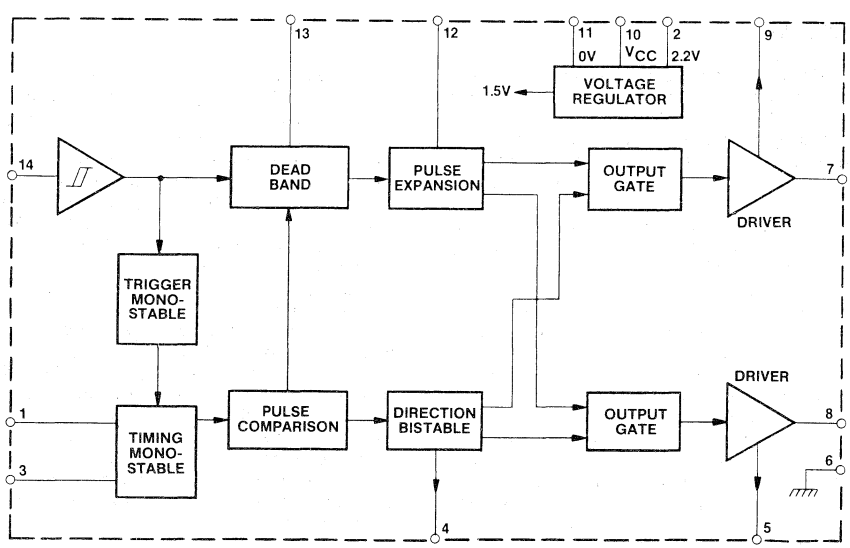


Fig.2 Block diagram for ZN409CE

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C, V_S = 5V

Characteristic	Value			Units	Test conditions
	Min.	Typ.	Max.		
Input threshold (lower)	1.15	1.25	1.35	V	Pin 14
Input threshold (upper)	1.4	1.5	1.6	V	Pin 14
Ratio upper/lower threshold	1:1	1:2	1:3		-10°C to +65°C
Input resistance	20	27	35	kΩ	
Input current	350	500	650	μA	
Regulator voltage	2.1	2.2	2.3	V	-10°C to +65°C, 1.3mA load current
Regulator supply rejection ratio	200	300	-		V_S = 3.5V to 6.5V $RSRR = \frac{dV_{IN}}{dV_{OUT}}$
Monostable linearity	-	3.5	4.0	%	±45°, R_P = 1.5kΩ, R_1 = 12kΩ
Monostable period temperature coefficient	-	+0.01	-	%/°C	Excluding R_T,C_T. R_P = 1.5kΩ, R_1 = 12kΩ (potentiometer slider set mid-way)
Output Schmitt deadband	±1	±1.5	±3	μs	C_E = 0.47μF
Minimum output pulse	2.5	3.5	4.5	ms	C_E = 0.47μF, R_E = 180kΩ
Error pulse for full drive	70	100	130	μs	15ms repetition rate C_E = 0.47μF, R_E = 180kΩ
Total deadband	±3.5	±5	±6.5	μs	C_D = 1000pF
PNP drive	40	55	70	mA	T = 25°C
	35	50	65	mA	T = -10°C
Output saturation voltage	-	300	400	mV	I_L = 400mA
Direction bistable output	2	2.8	3.6	mA	
Supply voltage range	3.5	5	6.5	V	
Supply current	4.6	6.7	10	mA	Quiescent
Total external current from regulator	1.3	-	-	mA	V_S = 3.5V
Peak voltage $V_{C\ EXT}$ (with respect to 2V regulated voltage)	-	0.7	-	V	T = 25°C
	-	0.5	-	V	T = -10°C

CIRCUIT DESCRIPTION

The ZN409CE incorporates a precision, dual voltage source providing 1.5V for internal use and 2.2V for external circuit requirements.

The input circuit is a Schmitt trigger allowing servo operation independent of edge speed, as obtained from the receiver-decoder.

Output from the Schmitt trigger is fed to the deadband and monostable circuits. The deadband circuit provides a programmable area of insensitivity to input pulse in order to eliminate hunting and overshoot. Dynamic feedback can be used to reduce the width of the deadband to acceptable levels, and to maintain correct servo operation.

The monostable circuits provide the inputs to the pulse comparison circuit which determines direction and amount of drive required to reach the new position. The output drive is also controlled by the pulse expansion circuit. This circuit ensures that a stationary motor will start rotating without drawing full stall current. This gives much improved battery life.

ZN410E

MOTOR SPEED CONTROLLER CIRCUIT

The ZN410E is a monolithic silicon integrated circuit which has been developed to offer a low cost speed controller of universal motors (AC series). The circuit contains all the functions required for the phase control of universal motors in closed loop systems. It incorporates a tacho input designed for a magnetic coil pickup and the IC requires a minimum of external components.

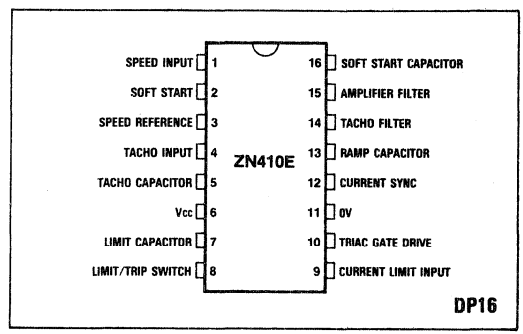


Fig.1 Pin connections - top view

FEATURES

- Direct Supply from AC Mains or DC Power Source
- Low External Component Count
- On-Chip Shunt Regulator
- Soft Start Ramp Circuit
- Optional Current Limit or Trip
- Magnetic Pickup Tacho Input
- Circuit Reset on Power Down
- Guaranteed Full Cycle Conduction with Inductive
- Load
- Negative Firing Triac Pulses
- Low Cost

ABSOLUTE MAXIMUM RATINGS

Shunt regulator current	25mA
Input voltage (pin 9 w.r.t. pin 6)	+5V max.
	-5V min.
Maximum input current (pins 4, 12)	±2mA
Output voltage (pin 10)	+7.5V max.
	-0.5V min.
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

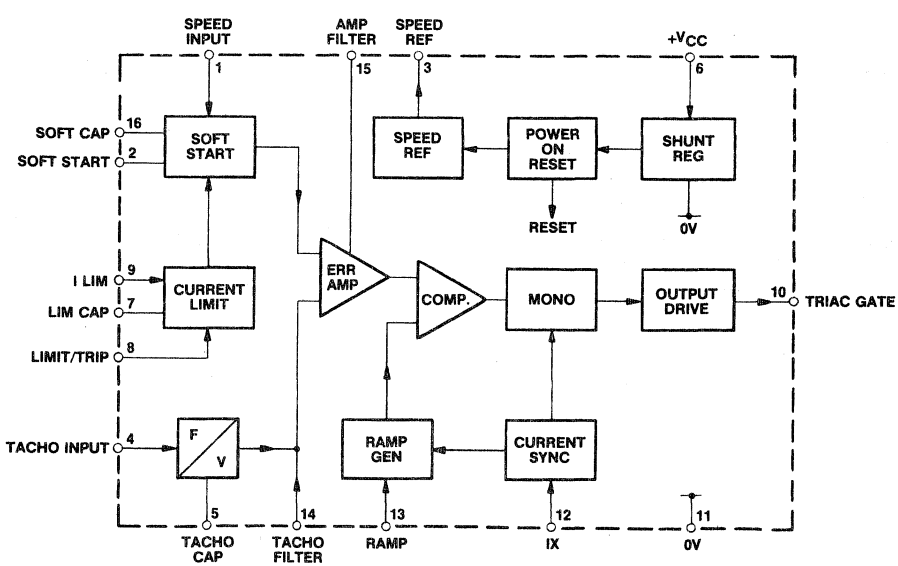


Fig.2 Block diagram of ZN410E

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage regulator					
Shunt regulator voltage (V_{REG})	4.7	-	5.6	V	I_{CC} = 5.5mA
Shunt regulator slope resistance	-	-	20	Ω	I_{CC} = 5.5mA
Supply current	3.5	-	25	mA	
F/V converter					
Tacho input threshold voltage	-	±100	-	mV	
Tacho input current	-	500	-	nA	$V_{pin\ 4} = V_{CC}$
Tacho maximum input frequency	20	100	-	kHz	
Speed control					
Speed reference voltage (w.r.t. pin 6)	-	-1.28	-	V	I_{IN} = 12.8μA
Speed reference input current	-	-	25	μA	
Speed input voltage range (w.r.t. pin 6)	$-V_{pin\ 3}$	-	0	V	
Speed input current	-	0.05	1.0	μA	$V_{pin\ 1}$ = 5.0V
Soft start capacitor charge current	5.3	7.5	12.0	μA	
Current limit					
Current limit input threshold	(330)	425	465	mV	½ cycle mean AC
Limit capacitor time constant	75C	150C	300C	ms	$C_{pin\ 7}$ in μF
Current sync					
Current sync threshold current	-	±120	±165	μA	
Current sync asymmetry	-	-	±10	μA	
Current sync clamp voltage (w.r.t. pin 6)	-	±1450	-	mV	I_{IN} = ±1mA
Ramp generator					
Ramp input charge current	35	50	70	μA	V_{IN} = 0V w.r.t. pin 6
Ramp input optimum max. negative level	-	-1.45	-	V	w.r.t. pin 6
Ramp input discharge voltage		-0.75	-	V	w.r.t. pin 6
Ramp input discharge current	-	10	-	mA	$V_{pin\ 13}$ = -1.45V (w.r.t. pin 6)
Triac gate drive					
Output current (on state)	65	100	130	mA	$V_{pin\ 10}$ = 2.0V
Output current (off state)	-	-	20	μA	$V_{pin\ 10}$ = 5.0V
Output pulse width	50	100	150	μs	R_L = 100Ω, 50% level
Error amplifier					
Phase angle/error voltage relationship ($V_{pin\ 1}$ - $V_{pin\ 14}$)	-	2	-	°/mV	Ramp $V_{pin\ 13}$ = 500mV
Tacho filter input voltage range (w.r.t. pin 6)	-	-	-1.5	V	
Amplifier filter time constant	35C	50C	65C	ms	$C_{pin\ 13}$ in μF

CIRCUIT DESCRIPTION (See Fig.2)

The basis of operation of the ZN410 is that two signals representing the demanded motor speed and actual motor speed are compared and the difference signal is used to define the conduction angle of a triac controlling the AC supply to the load. The speed demand signal is a voltage level input derived from a potentiometer connected between the positive supply rail and an on-chip reference voltage at pin 3. Zero speed corresponds to the pot wiper at the positive rail and maximum speed to the wiper at pin 3 end. The IC is designed to operate with a potentiometer of nominally 100kΩ.

The actual speed signal is an alternating voltage connected to pin 4, usually derived from a magnetic pickup type tacho with the magnetic rotor mounted on the motor armature, where the signal frequency is directly proportional to the angular velocity of the armature. The tacho signal is converted to a d.c. voltage level by the Frequency to Voltage converter stage. This voltage is compared with the signal from the speed potentiometer, and the difference signal is amplified by the Error Amplifier, the output of which is fed to the one input of the Ramp Comparator. A reference sawtooth ramp signal which is synchronised to the AC mains cycle is fed to the other comparator input. The point in the mains cycle where these two signals coincide defines the firing point for the triac. The Ramp Comparator output triggers a Monostable circuit which defines the gate pulse width for the triac. This signal is buffered to produce a negative going constant current pulse on the Triac Gate Drive output, pin 10, suitable for most low-medium power triacs.

The circuit together with the motor and tacho form a closed loop system which attempts to keep the motor speed constant irespective of changes in the mechanical loading on the motor. For example as the load increases the motor speed will tend to drop. This is refelected as a reduction in frequency of the tacho signal on pin 4 and produces a corresponding positive going rise in voltage at the f/V output on pin 14. The Error Amplifier amplifies this to produce a much larger increase in voltage at the inverting input of the Ramp Comparator. The sawtooth reference timing ramp fed to the non-inverting comparator input is a negative going slope which starts shortly after the mains cycle crosses zero. Hence the comparator output will now switch low earlier in the mains cycle resulting in an increase in the triac conduction angle, thereby applying more power to the motor in an attempt to maintain the original speed. In actual fact due to the finite gain of the system a reduction in speed with increased load is inevitable, otherwise the system would be unstable. This is a measure of the speed regulation of the system. The circuit gain could be increased to improve the regulation, but a point is reached where, dependent upon the mechanical dynamics of the system it becomes unstable. Hence a compromise has to be found between speed regulation and dynamic performance.

The ZN410 features an on-chip shunt regulator which allows operation of the IC directly from the AC mains supply in conjunction with either a resistive or reactive dropper. A soft-start function is also incorporated, the purpose of which is to produce a smooth acceleration of the motor whenever the power is applied or the speed input is rapidly increased. In association with the Power-On Reset circuit this function performs a controlled power-up sequence whenever the supply is interrupted. The Current Limit circuit senses the load current via a low value series resistor in the motor circuit. This signal is integrated to produce a level proportional to the average load current, and can either limit the load current by reducing the triac condition angle hence providing a constant current/torque characteristic, or it provides a trip function which removes power to the load by inhibiting the Triac Gate output. The inhibit is held on until the Power-On Reset circuit is activated by interrupting the IC supply.

PLESSEY
Semiconductors

ZN411

PHASE CONTROL INTEGRATED CIRCUIT

The ZN411 is a monolithic silicon integrated circuit designed primarily for the purpose of closed loop speed control of Universal Motors for use in power tools, food mixers, vacuum cleaners etc. The IC will also function in open loop and with both resistive or inductive loads in a multiplicity of phase control applications.

FEATURES

- Direct Supply from AC Mains or DC Power Source
- Soft Start Ramp Circuit
- Negative Triac Firing Pulses
- Triac Retrigger Facility
- Current Limit
- Tacho Input Compatible with Hall Effect Switch Devices
- Electronic Interlock and Speed Limit in Reverse Mode

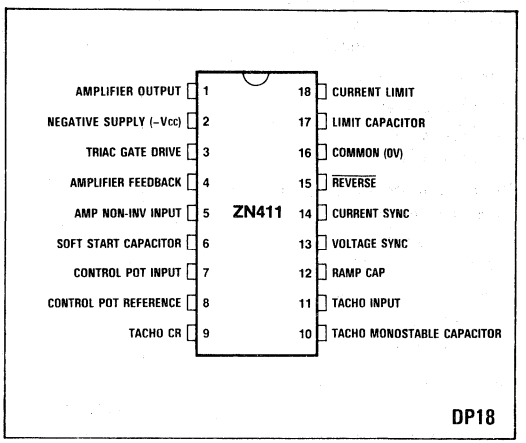


Fig.1 Pin connections

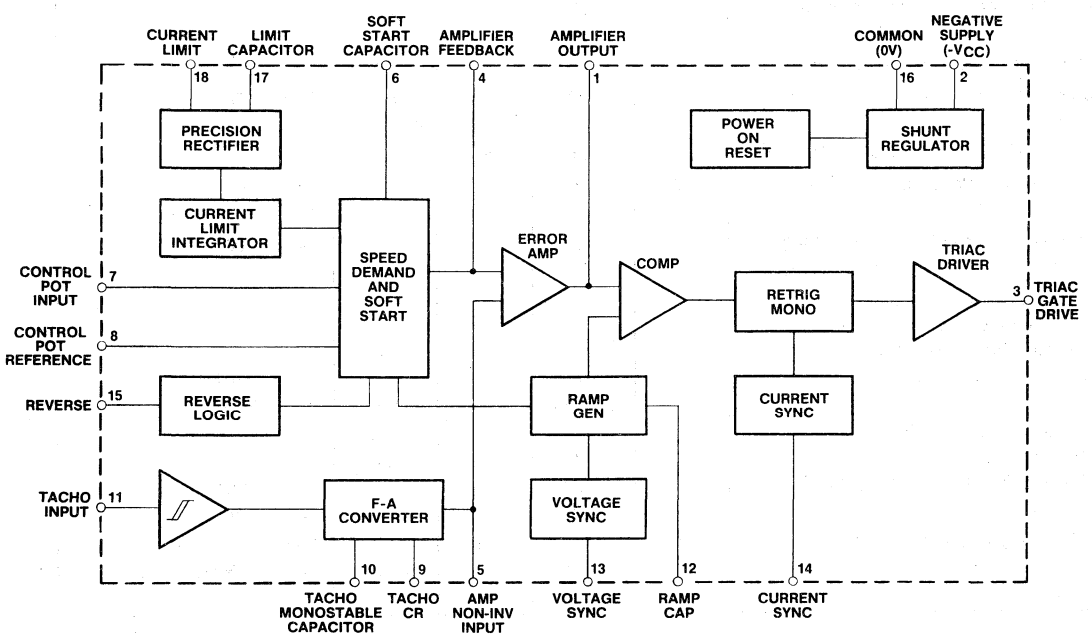


Fig.2 Block diagram of ZN411

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C. All voltages measured w.r.t. 0V Pin 16.

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Minimum operating voltage		-4.5		V	
Supply current I_{CC}		-4.0	-8.0	mA	$-V_{CC}$ = 4.5V All other pins O/C
Shunt regulator voltage V_S	-4.75	-5.1	-5.4	V	I_{CC} = 10mA
Shunt regulator slope resistance		4.0	10.0	Ω	I_{CC} = 10mA
Rev input threshold voltage					
Pin 15 V_{TH} High State		2.9	3.4	V	
V_{TL} Low state	1.1	1.3	1.7	V	
(w.r.t. $-V_{CC}$ Pin 2)					
Rev input current Pin 15					
I_{IH} High state		150		μA	V_{IN} = 0V
I_{IL} Low state			-1	μA	$V_{IN} = -V_{CC}$
Tacho input threshold voltage Pin 11					
V_{TH} High state		2.9		V	
V_{TL} Low state		1.3		V	
(w.r.t. $-V_{CC}$ Pin 2)					
Tacho input current Pin 11					
I_{IH} High state		20		μA	V_{IN} = 0V
I_{IL} Low state		-125		μA	$V_{IN} = -V_{CC}$
Control input voltage range Pin 7	V_{p8} (Note 1)		0	V	RV1 = 100k Pin 15 = 0V
Control input voltage range Pin 7 - Reverse mode	0.23V (Note 1)		0	V	RV1 = 100k Pin 15 = $-V_{CC}$
Control input current Pin 7		100		nA	V_{IN} = 0V
Control potentiometer input bias current Pin 8		20		μA	
Soft start capacitor charge current Pin 6		10		μA	
Current limiting input threshold voltage Pin 18		540		mV mean AC	C7 = 470nF
Error amplifier open loop DC voltage gain	29	40	51		
Error amplifier closed loop AC voltage gain	2.9	4.4	5.0		C3 = 220nF R1 = ∞ f = 1kHz
Minimum error amplifier output voltage		-3.4		V	RV1 = 100k
Maximum error amplifier output voltage		0		V	
Voltage sync input, Pin 13					
Positive input threshold current		42		μA	
Negative input threshold current		14		μA	
Clamp voltage (w.r.t. $-V_{CC}$)		+1.4		V	I_{IN} = +1mA
		-100		mV	I_{IN} = -1mA
Current synch. input Pin 14					
Threshold current		±110		μA	
Clamp voltage (w.r.t. $-V_{CC}$)		+1.4		V	I_{IN} = +1mA
		-100		mV	I_{IN} = -1mA
Timing ramp amplitude, Pin 12	1.5	2.0	2.8	V pk-pk	Supply frequency at Pin 13 = 50Hz C5 = 1μF

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Value			Unit	Conditions
		Min.	Typ.	Max.		
Timing ramp capacitor charge current Pin 12		15	20	28	μA	
Triac gate pulse output Pin 3 output voltage (V_G)		-3.5			V	R_{LOAD} Pins 3-16 = 68Ω
Output current (On state)	(I_G)	80	110	140	mA	V_{OUT} = -3V
Output current (Off state)	(I_G)			20	μA	V_{OUT} = 0V
Output pulse width (t_G)		40	80	150	μs	
Minimum tacho input pulse width Pin 11			10		μs	

NOTE
1. V_{P8} = Voltage measured at pin 8 with RV1 = 100kohms. Typically = -2V.

ABSOLUTE MAXIMUM RATINGS

All voltages measured with respect to -V_{CC} Pin 2.

Maximum shunt regulator current	25mA
Input voltage on pins 15 and 18	Maximum 7.5V Minimum -0.5V
Maximum input current on pins 13 and 14	±2mA
Output voltage on pin 3	Maximum 7.5V Minimum -0.5V
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

CIRCUIT DESCRIPTION

The ZN411 basically operates by comparing a voltage set on a potentiometer, proportional to speed demand, with a voltage derived from a frequency to voltage converter, proportional to motor speed. This difference or error voltage is amplified and used to define the conduction angle of a triac connected in series with the motor supply.

The input to the Frequency to Analog (F-A) converter is normally a signal from a tacho generator connected directly to the motor, the output frequency of the tacho being proportional to motor speed. The two voltages representing speed demand and motor speed are subtracted and the results amplified by the Error Amplifier, the output of which is connected to one input of the Ramp Comparator. The other input to the Comparator is driven from the Ramp Generator with a negative going sawtooth waveform which is synchronised to the signal on the Voltage Sync input, normally the 50Hz mains. The ramp is allowed to start shortly after the mains voltage passes through zero volts. When the ramp voltage becomes more negative than the Error Amplifier output then the Comparator output switches low and triggers a Retriggerable Monostable, which via the Output Drive Buffer will fire the Triac with a negative going current pulse. The firing angle of the triac will be dependent on the difference between the speed demand and the actual motor speed. Hence if the speed falls due to increased mechanical load, then the F-A output will go more positive, driving the Error Amplifier output positive also. The Ramp voltage will now charge to a voltage equal to the Amplifier output in a shorter time resulting in the triac gate pulse occurring at an earlier time in the mains half cycle, and consequently more power will be applied to the motor to maintain a constant speed.

When driving inductive loads, with a lagging phase angle, at or near to full conduction angle, it is necessary to ensure that the load current from the previous half cycle has fallen to zero and the triac switched off, before applying the next triac gate pulse. This is accomplished by means of the current crossing sense input which actually monitors the voltage on the live side of the triac. This input is also used to retrigger the Monostable by detecting if, for some reason due to interruptions of the load current (e.g. brush bounce), the triac inadvertently switches off during the conduction phase.

A soft start function is provided at switch-on by ramping the speed demand voltage in a negative direction at a constant rate up to a level dependent on the voltage on the Control input. This ramp is reset whenever the supply to the ZN411 is interrupted. The switch-on reset circuit also inhibits the Output Drive Buffer until the ZN411 supply has reached operating level.

The current limit circuit operates on the average current level flowing in the load. This is achieved by monitoring across a low value resistor connected in series with the load. This signal is rectified by a precision half wave rectifier and the negative cycles fed to an integrator. The output from this integrator feeds one input of a threshold comparator, the other input of which is maintained at a fixed reference level. When the voltage output from the integrator exceeds the reference level the comparator switches and the output is used to reduce the speed demand level until the average load current drops below the set limit. In effect the motor output changes from a constant speed to a constant torque characteristic.

The reverse logic is activated by detecting a change in logic state (i.e. Low to High or vice versa) at the REV input pin. When this occurs the Soft Start Ramp is reset, removing the Triac gate drive until the motor speed, as detected by monitoring the output falls to almost zero. At this point the reset is removed allowing the Soft Start Ramp to commence. With the REV input low the speed demand signal level is clamped to nominally 25% of its full scale range. The purpose of this is to limit the maximum speed of the motor in the reverse direction, primarily to minimise wear on the brush gear and commutator. For normal applications the reverse switch would be one-pole of a three-pole changeover used to reverse the connections to the armature.

ZN1060E

SWITCH MODE REGULATOR CONTROL CIRCUIT

The ZN1060E is a silicon integrated circuit designed as a general purpose switching regulator controller. The circuit incorporates all the control and protection functions required in a switched mode power supply. It can also be used in a variety of power control applications such as dc/dc converters and motor speed control.

The ZN1060E has been characterised for operation over the temperature range -20°C to +85°C.

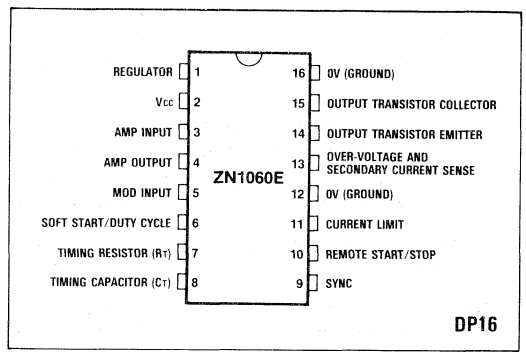


Fig.1 Pin connections - top view

FEATURES

- Stabilised Power Supply
- Low supply voltage Protection
- Linear Pulse Width Modulator
- Programmable Duty Cycle
- Programmable Soft Start
- Double Pulse Suppression
- High Speed Current Limiting
- Loop Fault Protection
- Uncommitted Error Amplifier
- Overvoltage Protection
- Remote On/Off Switching
- Secondary Current Monitoring
- Multiple Device Synchronisation
- Core Saturation Protection

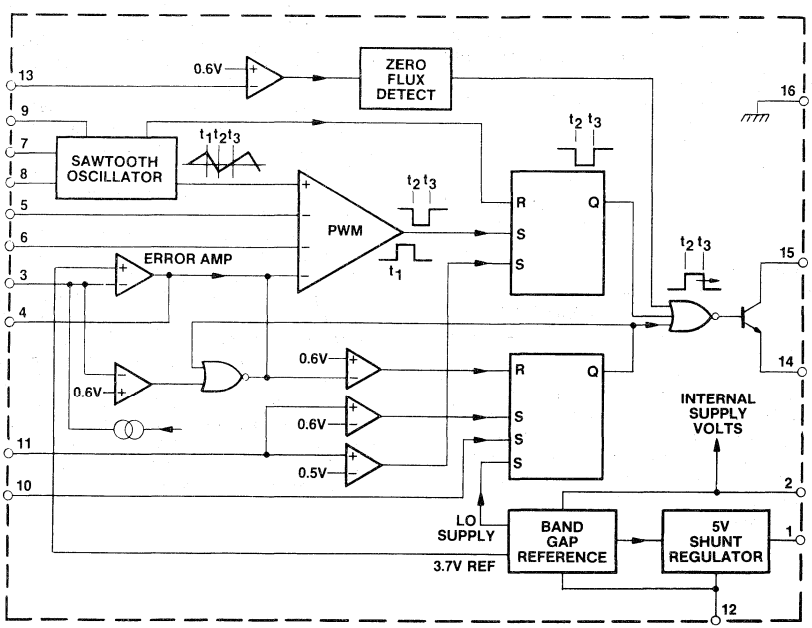


Fig.2 Block diagram of ZN1060E

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C, V_{CC} = 5V

Characteristic	Symbol	Value			Units	Test conditions
		Min.	Typ.	Max.		
Reference section						
Output voltage	V_{REF}	4.75	5	5.30	V	I_C = 20mA
Slope resistance	R_S	-	2	4	Ω	
Temperature coefficient	TC	-	100	-	ppm/°C	
Amplifier section						
Open loop gain	A_O	-	60	-	dB	
Input bias current	I_3	-	4	40	μA	
External feedback resistor	R_{3-12}	100	-	-	kΩ	
Reference voltage	V_{REF}	3.42	3.72	4.03	V	
Reference temperature coefficient	$\Delta V_{REF}/\Delta T$	-	100	-	ppm/°C	
Output voltage swing positive	V_{oh}	3	-	-	V	
Output voltage swing negative	V_{ol}	-	-	0.4	V	
Oscillator section						
Frequence range	f	50	-	100k	Hz	
External capacitor	C_T	1	-	-	nF	
External resistor (pin 7)	R_T	10	-	40	k	
Duty cycle range		0	-	98	%	
Sawtooth Upper level	V_{RH}	-	3	-		
Lower level	V_{RL}	-	1.1	-	V	
Modulator						
Modulator input current	I_{5-12}	-	4	40	μA	Voltage on pin 5 = 1V
Protection functions						
Pin 6 duty cycle limit control	V_6	39	41	43	% of V_Z	For 50% max. 15 to 50kHz
Pin 6 input current	I_{6-12}	-	0.5	20	μA	V_{IN} = 2V
Pin 1 low supply voltage protection threshold	V_{LT}	3.5	4	4.5	V	
Pin 3 feedback loop trip on threshold	V_{3-12}	472	600	720	mV	
Pin 3 pull up current	I_3	-	15	35	μA	
Pin 13 demagnetisation/overvoltage trip on threshold	V_{13-12}	-	600	-	mV	
Pin 13 input current	I_{x13}	-	1.3	5	mA	V_{IN} = 2V
External synchronisation						
Pin 9 Off	V_{9-12}	0	-	0.8	V	
On		2	-	5.25	V	
Sink current	I_{9-12}	-	-	100	μA	
Remote On/Off						
Pin 10 On	V_{10-12}	2	-	5	V	V_{CC} = 5V
Off	V_{10-12}	0	-	0.8	V	
Sink current	I_{10-12}	-	-	100	μA	V_{11-12} = 250mV
Current limit						
Pin 11						
Current limit	V_{11-12}	0.40	0.48	0.58	V	
Shutdown/slow start	V_{11-12}	0.47	0.60	0.72	V	
Sink current	I_{11-12}	-	-	450	μA	
Output stage						
Output current pin 15	I_{15}	40	-	-	mA	
Maximum emitter voltage pin 14	V_{14-12}	-	-	5	V	
Collector saturation voltage pin 15	V_{15-12}	-	0.4	-	V	
Supply current		-	12	20	mA	V_{1-12} = 5V

ABSOLUTE MAXIMUM RATINGS

Dissipation	350mW
Output current sink	40mA
Collector supply voltage	6V
Operating temperature range	-20°C to +85°C
Storage temperature range	-55°C to +150°C

THERMAL CHARACTERISTICS

Chip to case θ_{JC}	65°C/W
Chip to ambient θ_{JA}	110°C/W

CIRCUIT DESCRIPTION

Power Supply

The ZN1060E provides an on-chip 5V shunt regulator and an internal precision voltage reference (temperature compensated).

Start-Stop Circuit

In multiple power supply applications it is often necessary to control the on-off sequence logically. This is easily achieved with the ZN1060E by making use of the remote start-stop circuit.

Taking pin 10 below 0.8V will inhibit the output whereas allowing pin 10 to float or taking it to 2V or over enables the output.

Soft-Start

A soft-start function can be achieved by programming the duty cycle controller via pin 6.

Error Amplifier

The output voltage is controlled with the error amplifier in the feedback loop. The internal precision voltage is used as a reference.

Oscillator

This device provides an internal sawtooth oscillator with a programmable frequency range of 50Hz to 100kHz. If required it may be synchronised to an external clock.

Pulse Width Modulator

The ZN1060E provides a linear trailing edge PWM with double pulse suppression.

Protection

Using on-chip comparators and the internal reference voltage the ZN1060E offers zero flux detection, overcurrent monitoring with automatic reset, and feedback loop trip.

PLESSEY
Semiconductors

ZN1066E/J

SWITCHING REGULATOR CONTROL AND DRIVE UNIT

The ZN1066 is designed to satisfy the requirement for a general purpose control and drive unit in switching power supplies, transformer coupled DC/DC converters, transformerless voltage doublers, polarity converters, motor speed control and other power control applications.

FEATURES

- Complete PWM Power Control Circuitry
- Single Ended or Push-Pull Totem Pole Type Outputs with ±120mA Capability
- 0-100% Duty Cycle Control
- Feedback Control Guarantees Non-Overlap of Output Pulses
- No Dead Time Setting Required
- Output Frequency Adjustable up to 500kHz
- Independent Control of Output Voltage and Output Current
- 2.6V Stable Reference ±50ppm/□C
- Inhibit and Synchronising Input

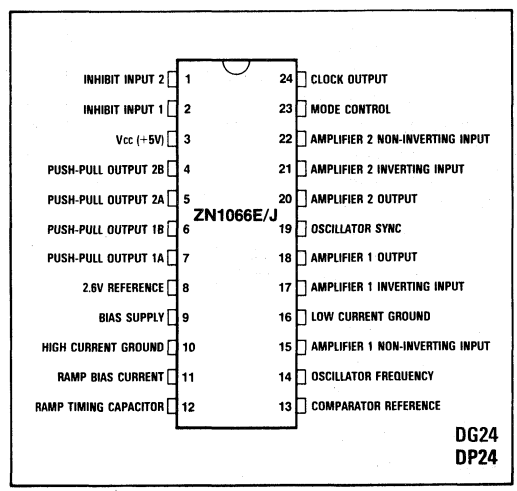


Fig.1 Pin connections - top view

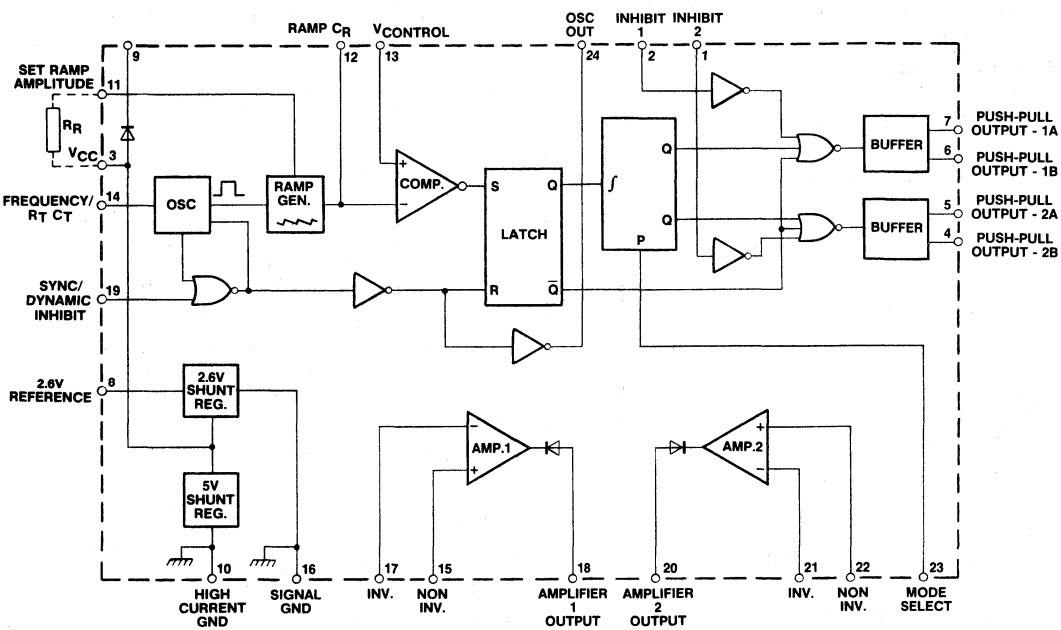


Fig.2 Block diagram of ZN1066E/J

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25 °C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulator section					
Output voltage (I_{CC} = 60mA)	4.75	5.0	5.25	V	See Notes 1 and 2
Voltage temperature coefficient (I_{CC} = 60mA)	-	100	-	ppm/°C	
Output impedance	-	1.5	3	Ω	
Supply current	-	40	-	mA	Shunt regulator just on
Amplifier section					
Open loop voltage gain	800	1200	-		
Input bias current	-	1	4	μA	
Input offset current	-	0.2	2	μA	
Input offset voltage	-	2	5	mV	
Offset voltage temperature coefficient	-	10	-	μV/°C	
Output low (sinking 1mA)	-	0.85	-	V	
Output high (sourcing 0.1mA)	4.7	-	-	V	With 1k pull up
Output impedance	-	5	-	kΩ	
Common mode range	1	-	2.8	V	
Comparator section					
Common mode range	1	-	4.3	V	
Delay to output drive (±50mV input)	-	0.17	0.3	μs	
Delay to output drive (±10mV input)	-	0.2	-	μs	
Input bias current	-	1	4	μA	
Input offset current	-	0.2	2	μA	
Reference section					
Reference voltage (at 1mA source)	2.4	2.55	2.7	V	See Notes 3 and 4
Temperature coefficient	-	50	-	ppm/°C	
Output impedance	-	1.5	-	Ω	
Mode control section					
Single ended operation control input logic '1' (outputs 1A and 1B)	2.4	-	-	V	May be connected direct to V_{CC}
Push pull operation control input logic '0' (all outputs)	-	-	0.4	V	0V or left open circuit
Cross couple inhibits section					
Input logic '1' enables outputs	-	0.07	0.2	mA	See Note 5
Input logic '0' inhibits outputs	-	-	0.4	V	
Oscillator section					
Maximum frequency range	5×10^{-4}	-	500	kHz	Minimum value of C_T = 1500pF
Initial accuracy	-	2	-	%	$R_T C_T$ constant
Temperature stability	-	1	-	%	Over temperature range -55 °C to +125 °C
Output pulse width	-	0.3	-	μs	C_T = 1500pF
Output logic '0' (sinking 10mA)	-	-	0.4	V	Buffered output pin 24
Output logic '1' (sourcing 1mA)	2.4	-	-	V	Buffered output in 24
Output section					
Output current	-	±60	-	mA	
Output logic '0' (sinking 60mA)	-	0.4	0.45	V	Each output
Output logic '1' (sourcing 60mA)	1.0	1.45	-	V	100mA max. under short circuit conditions
Total standby current					
V_{CC} at 2.5V, output current 4mA	-	17	-	mA	Operation from V_{REF} to V_{CC} is permissible
V_{CC} at 5V, with outputs open	-	40	-	mA	

NOTES
1. Decouple pin 3 to GND with 0.22microfarads as close to pins 3 and 10 as possible.
2. Pin 10 GND for 5V regulator and output buffers.
3. Decouple pin 8 to GND with 0.22microfarads minimum as close to pins 8 and 16 as possible. V_{REF} will supply 1mA maximum without additional bias. Maximum sink current is 10mA.
4. Pin 16 GND for oscillator, ramp generator, comparator, amplifiers and 2.5V reference.
5. The inhibit logic 1 current is the source current required to ensure digitally high operation. The base ground resistor is nominally 10kOhms. Catching diodes to the 5V rail are included on-chip.

ABSOLUTE MAXIMUM RATINGS

Electrical (at -55°C to +70°C)	
Supply current (I_{CC})	200mA
Main output drive currents	160mA total
Clock output current (sink)	25mA
Reference current (sink)	10mA
Ramp control current	1mA
Bais sourcing current	1mA
Thermal	
Operating temperature range:	
ZN1066J	-55°C to +125°C
ZN1066E	-40°C to +85°C
Storage temperature range	-65°C to +150°C

CIRCUIT DESCRIPTION

The ZN1066 incorporates shunt regulators which provide a 2.6V stable reference and a 5V stabilised rail.

The on-chip oscillator is externally programmable to give a period in the range 2 seconds to 2 microseconds. Also, it may be synchronised to an external clock by means of the OSCILLATOR SYNC input.

Pulse width modulation is carried out by a ramp generator and comparator circuit. Maximum and minimum pulse widths are easily programmed with resistors.

Two uncommitted, wideband, differential input voltage amplifiers are available on this device. They can be used for loop stabilisation, current and voltage control, current limiting and opto-isolation techniques.

In order to prevent output voltage overshoots and magnetising current imbalances in the power transformer primary a soft start function is required. This forces the output duty cycle to increase gradually following system power up or an inhibit command. A soft start and an inhibit function are easily implemented on the ZN1066.

Automatic overlap control is provided by the control logic. This removes the requirement for dead time settings, and allows up to 100% output pulse widths. This ensures that the conflict between safe minimum off time and maximum control range no longer exists.

The ZN1066 provides four push-pull totem pole type outputs. This is the most flexible and versatile output configuration available. Each is capable of sinking or sourcing 60mA. They may be paralleled in order to provide increased drive.

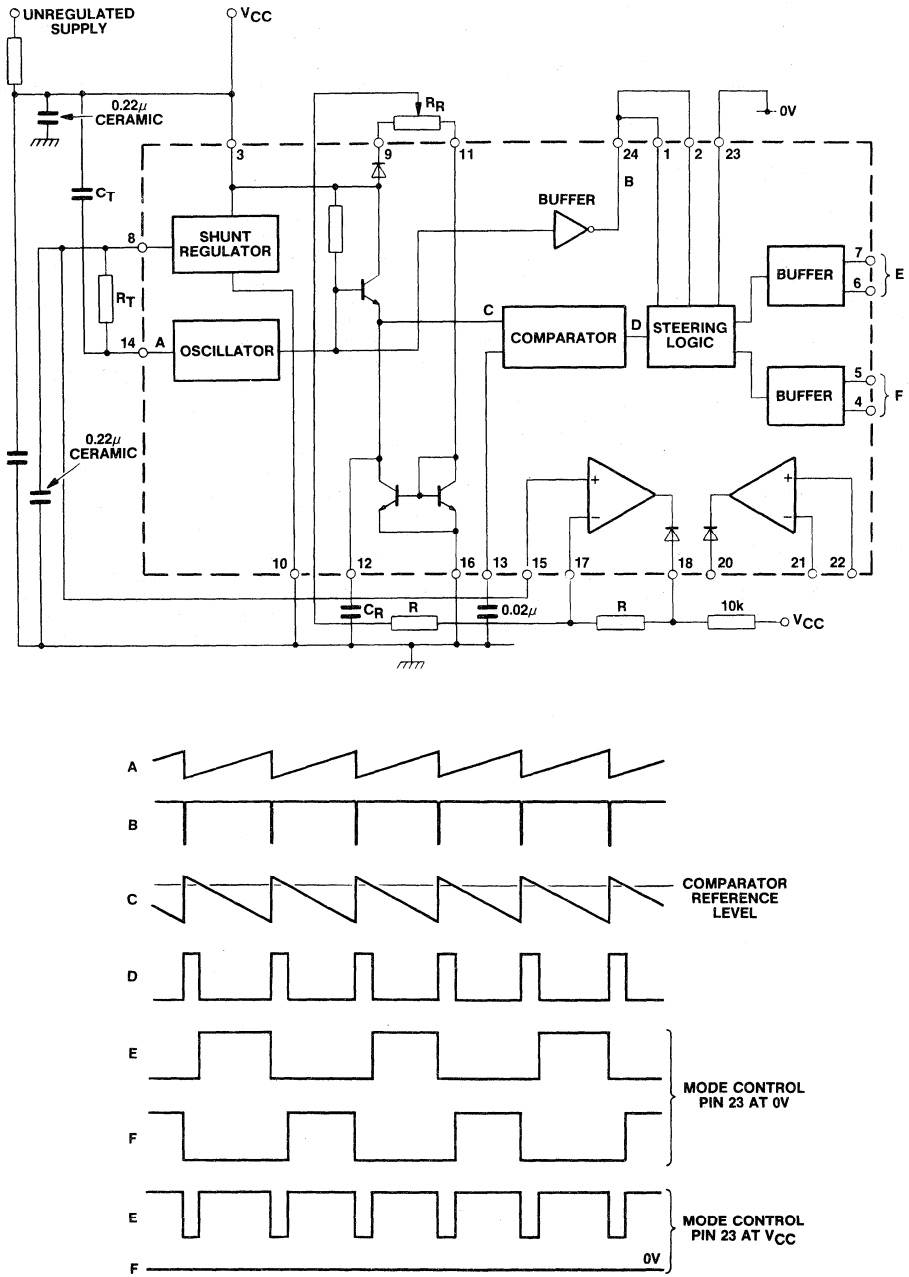
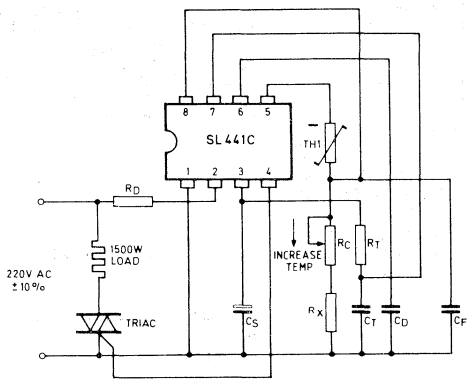


Fig.3 Open loop test circuit and system waveforms

Application Notes

An Electronic Thermostat for Room Heaters using the SL441C

The circuit in Fig.1 has a sensitivity of nominally 100mV/°C. The width of the proportional control band is nominally 1.0 °C and offers a good compromise between temperature stability and regulation performance. For potentiometer control characteristics see Figs.2 and 3.



SUGGESTED VALUES

R_D	8.2kΩ 5% 6W (less in air stream)	
R_C	22kΩ linear control potentiometer	
R_t	2.7MΩ	} Ramp period = 11 secs.*
C_t	4.7µF 10V TANT	
C_f	47nF (filter if required)	
C_S	150µF 16V	
C_D	2.2nF ±10%	
Triac	TAG 250-400	

TH1 NTC thermistor. R_{25} = 10kΩ
B = 4200. e.g. ITT KQ103
R_x 6.2k ±5% fixed resistor or 10kΩ preset.
See control characteristics Figs. 7 and 8

*If on-off control is required, omit R_T and C_T and link pin 7 to pin 1.

*Fig.1 Application circuit for proportional control system.**

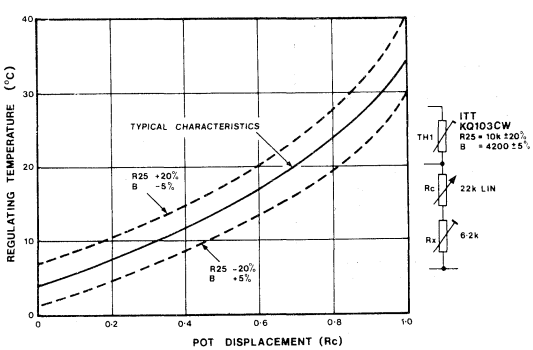


Fig.2 Control characteristics of electronic thermostat (mechanical calibration)

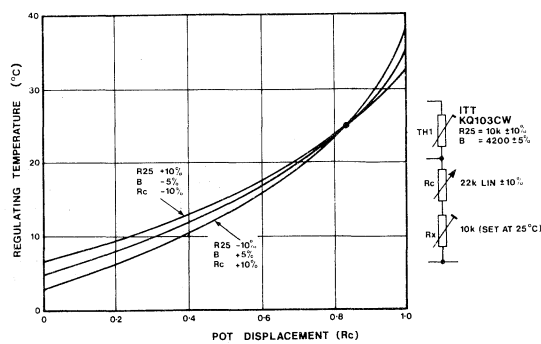
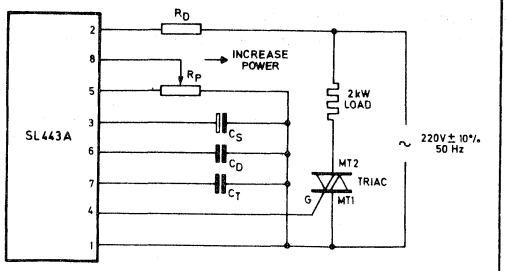


Fig.3 Control characteristics of electronic thermostat (electrical calibration)

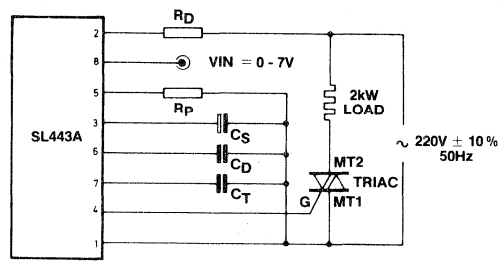
SL443A Application Circuits



Component values

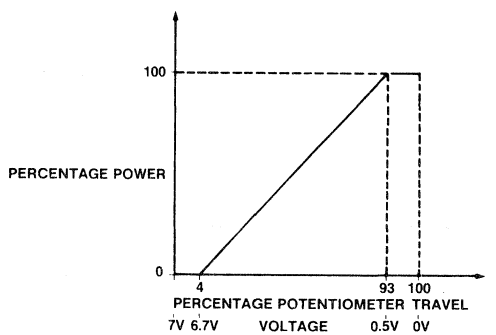
R_D 8.2kΩ 5% 7W
R_P 100kΩ (Control characteristic of linear potentiometer is shown in Fig.3)
C_S 220μF 16V
C_T 0.47μF (Ramp period = 20 seconds nominal)
C_D 1.5nF ± 10%
TRIAC TAG.255 - 400

Fig.1 Cooker hotplate control



Component values
R_D 8.2kΩ 5% 7W
R_P 100kΩ
C_S 220μF 16V
C_T 0.47μF (Ramp period = 20 seconds nominal)
C_D 1.5nF ±10%
TRIAC TAG.255 – 400

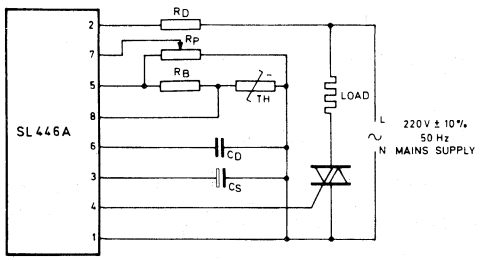
Fig.2 Voltage control



This characteristic applies to a linear potentiometer. Different control characteristics are easily obtained by using a non-linear potentiometer and/or offset resistors in the potentiometer circuit.

Fig.3 Output power v potentiometer displacement or voltage on pin 8

A Design Example using the SL446A



Components are to be standardised so that heating elements in the range 400 to 1200W may be used. The circuit is to provide linear temperature control over the domestic temperature range of +5°C to +35°C.

Fig.1 Space heater application of the SL446A

Triac selection

The minimum load resistance is $\frac{V^2_{RMS}}{P} = \frac{220^2}{1200} =$ 40.33Ω.

Assuming a manufacturing tolerance of ±5% in the load resistance, the maximum load current is

$$\frac{220 \times 1.1}{40.33 \times 0.95} = 6.32\text{A RMS}$$

The peak repetitive mains voltage is $220 \times 2 \times 1.1 =$ 342V Max.

A suitable triac is the TAG 245–400. This is an isolated triac with ratings of 400V and 6.5A RMS at a case temperature of +70°C. The device is suitable for positive gate pulse operation and requires an I_{GT} of 50mA at a V_{GT} of 2.5V for reliable triggering. These triggering requirements are easily met since the SL446A delivers more than 50mA into a 4V drain. The trigger pulse width should be ⩾ 20 μs (see below).

Capacitor C_D

This capacitor defines both the delay and width of the triac firing pulse. The triac can not latch until the mains voltage exceeds the sum of the triac on-state voltage V_T and V_H which is the voltage dropped across the load resistance by the triac holding current I_H. ($V_T = 2.0$, $I_H = 50$mA for the TAG 245). The maximum load resistance corresponds to the 400W element.

$$\frac{V^2}{P} = \frac{220^2}{400} = 121\Omega$$

Maximum load resistance $= 121 \times 1.05 = 127\Omega$

$V_H + V_T = 6.35 + 2 = 8.35\text{V} = V_L$, i.e., triac latching can occur at the 8.35V point in the supply cycle.

It is necessary, therefore, to ensure that the firing pulse does not finish before this point in the supply cycle.

$$\text{Using } t_f \geqslant \frac{V_L}{V_M \times \sqrt{2} \times 2\pi f}$$

(V_M is the minimum RMS mains voltage, f is the supply frequency.)

$$t_f = \frac{8.35}{220 \times 0.9 \times \sqrt{2} \times 2 \times \pi \times 50}$$

$$t_f = 95\,\mu\text{s}$$

Using t_f Min. $= 1.09 \times C_D \times$ R6 Min. (R6 Min $=$ 21.5kΩ)

$$C_D \quad \frac{95}{1.09 \times 21.5}\ \text{nF}$$

$$C_D \geqslant 4.05\text{nF}$$

Specify $C_D = 4.7\text{nF} \pm 10\%$ (Preferred value)

Using an ITT type KQ223Y thermistor in a bridge comprising $R_B = 18\text{k}\Omega \pm 2\%$ and $R_P = 22\text{k}\Omega \pm 20\%$ linear potentiometer, substantially linear temperature control is obtained over the domestic temperature range +5°C to +35°C. The output from the bridge is approximately 100mV/°C and since the SL446A has a hysteresis of 25mV in the servo amplifier, the hysteresis of the thermostat is typically 0.25°C. The maximum bridge supply current occurs when V_5 equals 9.0V; the thermistor is at the maximum temperature and the potentiometer resistance is at minimum.

The characteristics of the thermistor are:

$R_{25} = 22\text{K} \pm 10\%$

ß $= 4300 \pm 5\%$

Using $R_{T1} = R_{T2} \times e^{\left(\frac{ß}{T_1} - \frac{ß}{T_2}\right)}$ and inserting $R_{25} =$ −10% and ß = + 5% it is found that the resistance of the thermistor at 35°C (308°K) is 12.1k minimum.

$$I_5 = \frac{9}{22 \times 0.8} + \frac{9}{18 \times 0.98 \pm 12.1}\ \text{mA} =$$

0.814mA Max.

Average gate drive current I_4 (AV)

The maximum drive current is 200mA into a short circuit and this occurs for a period $2 \times t_p$ every mains cycle. It is acceptable to use the nominal value of R6 in the formula:

I_4 (AV) $= 2 \times t_p \times f \times 200\,\text{mA}$ and $t_p = 0.69\,C_D R6$

$= 2 \times (0.69 \times 4.7 \times 10^{-9} \times 27 \times 10^3)\ 50 \times 200\,\text{mA}$

$= 1.75\text{mA}$

If C_D has a +10% tolerance.

I_4 (AV) $= 1.75 \times 1.1 = 1.925\text{mA}$ Max.

Mains dropping resistor R_D

The total supply current of the circuit is $7.0\text{mA} + I_5 + I_4$ (AV) $= 7 + 0.814 + 1.925 = 9.74\text{mA}$ Max.

$$\text{Using } R_D = \frac{\text{peak mains voltage} - V_3 \text{ Max.}}{\pi \times I_{3AV}}$$

$$R_D = \frac{220.0.9 \times \sqrt{2} - 16}{\pi \times 9.74} \text{ k}\Omega \text{ Max.}$$

$R_D = 8.63$ kΩ Max.
Specify $R_D = 8.2$ kΩ ±5% (Preferred Value)

$$\text{The power dissipated by } R_D \text{ is} < \frac{V^2_{RMS} \text{ Max.}}{R_D \text{ Min.}}$$

$$< \frac{(220 \times 1.1)^2}{8.2 \times 0.95 \times 10^3}$$

Maximum power dissipated by R_D is 7.5 W.

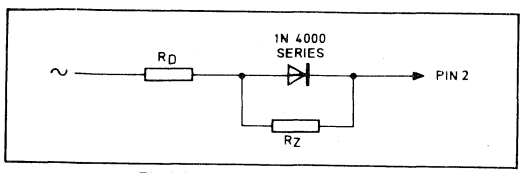


Fig.2 Mains supply input circuit

The power dissipated by R_D is approximately halved if a series diode is used. However, the diode must be shunted with a bypass resistor for proper operation of the zero voltage crossing detector circuit. Suggested values for the by-pass resistor are 39kΩ for 110, 220 and 240V applications and 82kΩ for 380V operation. The diode should be rated to withstand the peak mains voltage. In the design example, the peak mains voltage is 220 × 1.1 × 2 = 342V and a 400V device is suggested.

Supply smoothing capacitor C_S

$$\text{Using } C \geqslant \frac{1}{f} \times \frac{3}{4} \times I_{3AV} = \frac{3 \times 9.74 \times 10^3}{50 \times 4} \mu\text{F}$$

$C \geqslant 146$ µF.

Specify 220 µF −25%, +100%.

OPERATING NOTES

If any of the bridge components are distant from the IC additional spike filtering may be found necessary. An effective method is given below:

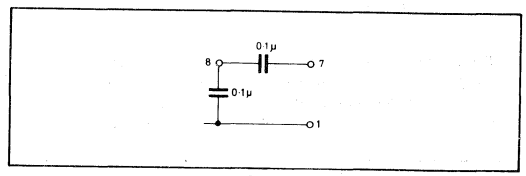


Fig.3

If the mains dropping resistor is mounted on the main printed circuit board, board capacitance can couple spikes directly to the circuitry. It is good practice, therefore, to place a guard ring around the circuitry and take this to the common line (neutral, pin 1).

Throughout this section, component references are those shown on the Reference System Circuit Diagram, Fig.1. See Table 1 for Symbol Definitions.

ANALOG FEEDBACK CONTROL

An anlog feedback voltage (V_f) of 0V to 13.5V, may be supplied directly to pin 4. With this type of feedback the frequency-to-analog conversion circuit should be made inoperative by connecting pin 12 to common (pin 8).

Motor speed sensing can be achieved by rectifying and smoothing a tachogenerator signal, thus generating directly an analog feedback control voltage. It is most important with this type of system that the tachogenerator does not pick up noise signals, particularly those generated by the motor field. This may well be a problem with simple tachos incorporated inside or close to the motor, by can easily be avoided by the use of digital sensing.

DIGITAL FEEDBACK CONTROL

In this type of feedback system the frequency of an input signal to pin 12 is converted to an analog feedback control voltage (V_f). Although digital sensing requires an extra couple of passive components it offers the advantage of not requiring any calibration of the machine, plus stability against ageing and temperature effects.

The zero voltage points of an AC tacho signal are sensed at pin 12.

Without diode D_2, the TDA1085C can function linearly with a range of tacho input signal levels between 0.2 and 6 volts. When D_2 is included, the device will function correctly, provided the positive tacho excursion does not exceed the open circuit tacho detection voltage (13.5 volts).

An over-voltage sensing circuit will reset the timing functions and inhibit triac drive pulses if the input exceeds 13.5 volts. Providing no resistive load is placed between pin 12 and common (pin 8), a 25μA tacho monitor bias current will cause the input pin voltage to exceed this limit if the tacho goes open circuit. By this means the TDA1085C is 'fail safe' in the event of tacho circuit failure.

Due to the inductive nature of a tacho pickup coil, the current output is proportional to the operating frequency. For a wide speed control range a predominantly frequency-independent voltage may be generated by integrating the pulses by means of a capacitor. C_3 performs this function; its value is dependent on the strength of the tacho signal.

Noise pickup by the tacho may be overcome by introducing an offset voltage (V_{to}) on the input. This is easily provided by R_9 and pin 12 bias current.

$$V_{to} = R_9 \times 25 \times 10^{-3} \text{ mV} \quad \ldots 1$$

R_9 also damps any resonance that may occur between C_3 and the tacho coil inductance.

Frequency to Analog Conversion

The F-A converter may be used to transform the frequency derived from a tacho drive to an analog voltage which is proportional to the motor speed. The tacho frequency is given by

$$f_t = \frac{SN}{120} \text{ Hz} \quad \ldots 2$$

Frequency to voltage conversion is achieved by integrating a pulse of charge (at pin 4) every time the tacho input (pin 12) goes positive. This unit of charge is defined by the capacitor connected to pin 11 (C_6) and is amplified by the circuit before being integrated at pin 4.

The conversion factor (K) is determined by C_6, R_{12} and the circuit gain (A_t), which may be calculated from

$$K = 10^3 (V_{cc} - 2V_{be}) A_t C_6 R_{12} \text{ mV/Hz} \quad \ldots 3$$

Simplifying gives

$$K \triangleq 14 \times 10^4 C_6 R_{12} \text{ mV/Hz} \quad \ldots 4$$

The analog feedback voltage (V_f) generated by the converter circuit is hence given by

$$V_f = Kf_t \times 10^{-3} \text{ volts} \quad \ldots 5$$

The maximum value of V_f which occurs at the highest motor speed should be designed to be $\leqslant$ 13.5 volts.

During charge transfer the internal impedance of pin 11 is approximately 100kΩ, hence the time constant of the transfer period is $10^5 C_6$ seconds. This time constant should be designed to be a fraction of the minimum positive tacho input pulse duration, in order to maintain a linear relationship between the tacho frequency and the resulting tacho feedback voltage.

C_5 is used to integrate the pulses on pin 4. To maintain linear operation of the control amplifier the ripple voltage (V_{fr}) should be made less than 200mV. Increasing the value of C_5 will reduce the ripple but will also increase the response time of the F-A converter. The ripple voltage may be calculated from

$$V_{fr} = \frac{10^3 A_t (V_{cc} - 2V_{be}) C_6}{C_5} \text{ mV} \quad \ldots 6$$

Simplifying

$$V_{fr} \triangleq \frac{14 \times 10^4 C_6}{C_5} \text{ mV} \quad \ldots 7$$

The temperature coefficient and performance may be improved by incorporating a 470kΩ resistor from pin 11 to V_{CC}. This will affect the conversion factor since this resistor will be competing with the internal (100kΩ) impedance of pin 11, for current from C_6. Due to this and other component tolerances, it may be necessary to calibrate the system by means of a variable resistor on pin 4. These components are shown incorporated in Fig.13b.

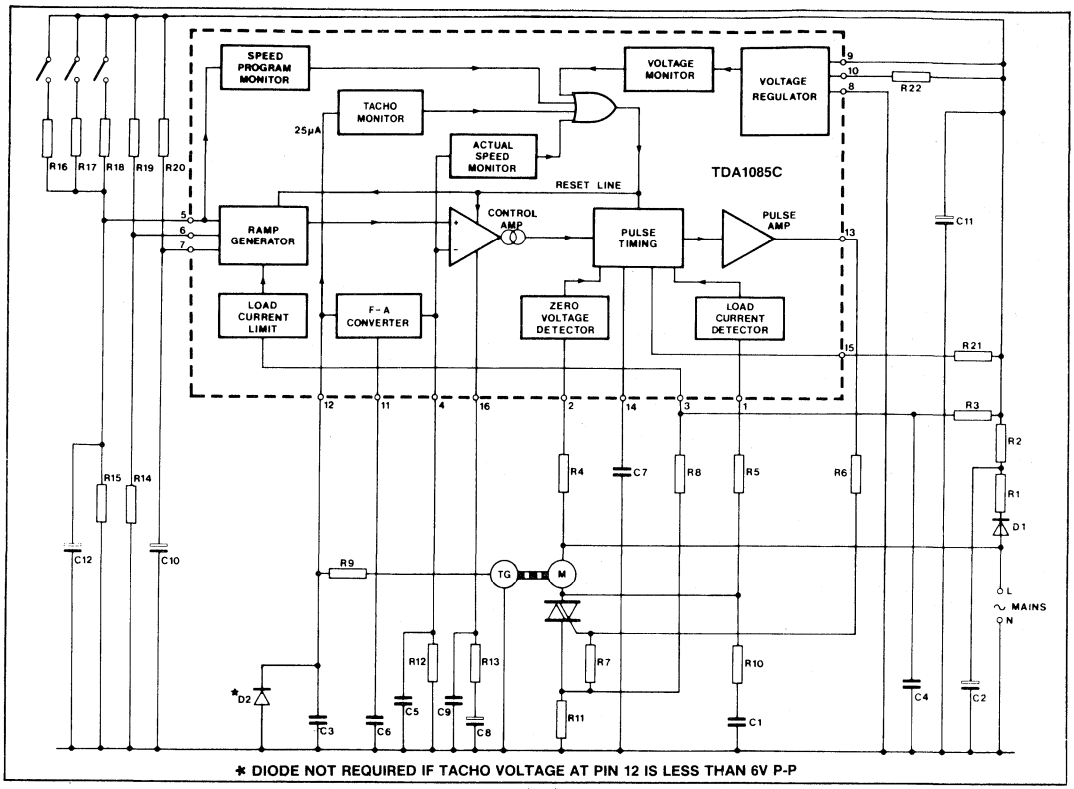
Provided the tacho input voltage at pin 12 is kept below 6V p-p then diode D2 is not required. If the tacho input voltage exceeds this, then a 1N4148 Si diode should be used to clamp the negative excursion at pin 12.

THE RAMP GENERATOR

The ramp generator's function is to limit the rate of change of the speed reference voltage (V_s) applied to the control amplifier. Providing this is the slowest time constant in a system, the amplifier will remain in a linear proportional control mode and prevent an excessive phase angle (or power) being applied to the motor load.

A programmable slow ramp period is available to enable a 'distribution period' to be provided in automatic washing machines, i.e. a controlled slow acceleration period where clothes are distributed evenly around a revolving drum prior to spin.

The ramp generator is a follower integrator design, hence the internal ramp voltage will only rise to the voltage programmed on pin 5. Due to the circuit design the ramp voltage seen on pin 7, is a V_{be} higher than the internal level at which it is monitored. If the speed program voltage is increased (e.g. from 'wash' to 'spin') then the transition is again determined by the ramp generator characteristic



* DIODE NOT REQUIRED IF TACHO VOLTAGE AT PIN 12 IS LESS THAN 6V P-P

Fig.1 Reference system circuit diagram

between the two programmed levels. Also if the motor speed is restrained by an overload then the internal ramp voltage is restricted from exceeding the analog feedback voltage (V_f) by more than V_{be}.

The fast ramp current (I_{rf}) is defined by the IC and is nominally 1.2mA. This current is integrated on pin 7 by C_{10}, to produce a linear ramp. Assuming the current provided by R_{20} is negligible compared to I_{rf}, the fast ramp rate (V_{rf}) is given by

$$V_{rf} = \frac{I_{rf}}{C_{10}} \text{ mV/s} \qquad \ldots 8$$

The knee voltages of the ramp (V_{ra} and V_{rb}) are dependent on the voltage programmed on pin 6 (V_6) (see Fig.3). These two levels define the speeds between which the motor will accelerate at the slow rate to provide a 'distribution period'. The relationships are

$$V_{rb} = 2V_6 \qquad \ldots 9$$

$$\text{For } V_6 \leqslant 1.2V,\ V_{ra} = V_6 \qquad \ldots 10$$

$$\text{For } V_6 \geqslant 1.2V,\ V_{ra} = 1.2V \qquad \ldots 11$$

During the distribution period the ramp rate is predominantly defined by the current provided by R_{20}. The average slow ramp rate (V_{rs}) may be calculated from

$$V_{rs} \triangleq \frac{2V_{cc} - 2V_{be} - V_{ra} - V_{rb}}{2R_{20}C_{10}} \times 10^3 \text{ mV/s} \qquad \ldots 12$$

Simplifying gives

$$V_{rs} \triangleq \frac{30 - V_{ra} - V_{rb}}{2R_{20}C_{10}} \times 10^3 \text{ mV/s} \qquad \ldots 13$$

The above expressions do not take account of the capacitor leakage current nor the residual charging current from pin 7. These parameters work against one another and therefore are self compensating to some extent. The leakage current of C_{10} should be specified at a voltage equal to $V_{rb} + V_{be}$.

The distribution period (T_d) may be calculated from

$$T_d = \frac{V_{ra} - V_{rb}}{V_{rs}} \times 10^{-3} \text{ s} \qquad \ldots 14$$

If a distribution period is not required, then pin 6 should be connected to common (pin 8). This circuit will then maintain a fast ramp up to the programmed speed voltage. A continuous slow ramp of exponential character can be provided by connecting pin 6 to pin 7. This maintains the circuit in a 'distribution' condition where the ramp is defined by R_{20} and C_{10}. Note that the bias current for pin 6 should be taken into account; it is expected to be less than $-10\mu A$ under these conditions.

SPEED PROGRAM VOLTAGE

The speed program voltage (V_5) on pin 5 must exceed the low threshold level of 80 mV. Timing functions will be reset and triac drive pulses will be inhibited if pin 5 is programmed below this level. The working range of V_5 is hence 80mV to 13.5 volts.

Pin 5 may be programmed by switching a resistor network to supply the required voltage levels. A small capacitor (C_{12}) may be required to prevent the ramp generator being reset due to pin 5 input going momentarily low.

THE CONTROL AMPLIFIER

The differential control amplifier is normally used to compare the analog feedback voltage (V_f), pin 4, with the internal speed reference voltage (V_s) and hence derive a phase control voltage (V_p) on pin 16. The amplifier has a transconductance gain of 300μA/V with a limited bidirectional output drive capability of $\pm$100μA. Hence proportional control occurs for a differential error input of $\pm$330mV.

The gain and phase compensation for closed loop control systems are determined by R_{13}, C_8 and C_9 connected to pin 16. These components are best chosen empirically to achieve a best compromise in terms of speed overshoot and response time.

For manual or open loop phase control, the control amplifier may be used as a buffer amplifier and use made of the ramp generator to control the rate of phase angle increase. This may be accomplished by connecting pin 4 to pin 16, grounding pin 12 to pin 8 and controlling the phase angle via the voltage applied to pin 5.

The maximum phase angle may be limited in both open and closed loop control systems by clamping the maximum voltage on pin 16 by means of a zener diode or other clamping device. Since there is only 100μA current drive from the control amplifier, it is important that the clamping device or circuit has a sharp turn-on knee.

During a reset condition pin 16 will be pulled low, ensuring that no output pulses are generated. When the inhibit signal is removed the phase angle increases from zero conduction at a controlled rate.

ZERO VOLTAGE DETECTOR

The sole purpose of the zero voltage detector is to reset the ramp generator of the pulse timing circuit at the zero voltage point of the mains cycle.

The AC mains is applied, via R_4, to a synchronisation circuit (pin 2) which produces a reset pulse whenever the input current is between $\pm$50μA. The pulse is symmetrical around the zero voltage points, which ensures that positive and negative wave triac conduction symmetry can be obtained.

R_4 should be chosen to limit the peak current drive to pin 2 to be slightly less than $\pm$1mA.

LOAD CURRENT DETECTOR

The load current detector inhibits triac gate pulses being generated by the pulse timing circuit until correct conditions exist for the triac to latch when fired. This condition exists when there is sufficient voltage across the triac to induce the required latching current within the duration of a firing pulse.

The triac voltage is monitored by means of R_5 in a similar manner to the zero voltage detector. In this case triac gate pulses are inhibited if the current into pin 1 is not greater than $\pm$50μA. Again the peak current drive should not exceed $\pm$1mA. From the above it follows that the minimum voltage across the triac when a gate pulse is supplied is given by

$$V_{tx} = R_5 \times 50 \times 10^{-6} \text{ volts} \qquad \ldots 15$$

TRIAC PULSE TIMING

The function of the pulse timing circuit is to control the delay and duration of the triac firing pulse. The pulse position is determined by resetting the ramp generator at the mains zero voltage points and triggering the pulse generating circuit when the ramp reaches a level determined by the phase angle control voltage on pin 16. With inductive loads the pulse may be further delayed by the load current detector circuit.

Full power may be supplied to inductive loads since when maximum conduction is demanded the triac pulse is delayed until the lagging load current from the previous half cycle has reduced to zero. At this point the triac will cease to conduct and the supply voltage will appear across it, which when detected initiates the next triac pulse.

At high motor speeds brush bounce may become severe and cause interruptions of the motor load current. Under these conditions the load current detector will respond to the supply voltage appearing across the triac and hence enable a retriggering pulse to be supplied.

The ramp waveform is generated by charging capacitor C_7 up to 12.8volts (nominal) during the zero voltage pulse determined by the zero voltage detector (pin 2). The charging current in this period is limited by an internal impedance of approximately 500ohms. After the zero voltage pulse, C_7 is discharged in a linear fashion by a current sink (I_d), defined externally on pin 15. When the voltage on C_7 reaches a value determined by the phase control voltage on pin 16 a triac gate pulse is initiated. The dynamic working range of this ramp generator is 11.7volts, i.e. the triac gate pulse may be created at any time before the ramp waveform has decreased by this voltage.

The triac pulse duration is determined by recharging C_7 with an internally defined current (I_r) to a voltage 100mV (nominal) above the original trip voltage. During this period the discharge current (I_d) is maintained and hence works against the charging current (I_r). Therefore, I_d must be smaller than I_r for the circuit to function as a pulse generator.

If retriggering occurs, the minimum delay will be determined by the time taken for the current I_d to discharge C_7 back to the original trip voltage i.e. back through 100mV. The maximum retriggering rate (t_r) is thus determined by this delay time plus the pulse duration.

Triac Pulse Timing Equations

Ramp discharge current

$$I_d = \frac{(V_{cc} - V_{be})}{R_{21}} \times 10^6 \ \mu A \qquad \ldots 16$$

Dynamic ramp voltage on pin 14

$$V_{rp} = \frac{I_d \times 10^{-6}}{2 \times f_m \times C_7} \text{ Volts} \qquad \ldots 17$$

Limitation on V_{rp} for full phase control

$$V_{rp} < 11.7 \text{ Volts} \qquad \ldots 18$$

TRIAC GATE PULSE

A triac pulse width of 50μs is suitable for most general purpose triacs. Standard component values for C_7 and R_{21} may hence be used which are as follows:

For 50Hz supply

$C_7 = 47\text{nF} \pm 10\%$
$R_{21} = 300\text{k}\Omega \pm 5\%$

For 60Hz supply

$C_7 = 47\text{nF} \pm 10\%$
$R_{21} = 270\text{k}\Omega \pm 5\%$

With the above components the retriggering period will be approximately 200μs

TRIAC GATE DRIVE

The triac gate pulse is amplified by a buffer amplifier that provides a positive low impedance emitter follower output drive to pin 13.

The current drive required will depend on the characteristics of the triac used. It is important to provide sufficient gate current to guarantee complete bulk conduction is achieved; if not, hot spots may occur which will reduce the life of the triac. The worst case condition is likely to exist when the device is fired in the fourth quadrant (i.e. positive current drive into the gate when a negative voltage is present on Main Terminal 2 (MT2) of the triac).

With sensitive triacs, R_7 may be required to provide a path for the output leakage current and make the triac less susceptible to false triggering from electrical noise.

The triac gate current drive may be calculated from

$$I_{tg} = \frac{V_{13} - V_{tg}}{R_6} - \frac{V_{tg}}{R_7} \times 10^3 \text{ mA} \quad \ldots 19$$

TRIAC LATCHING

As mentioned before, it is necessary to trigger the triac when conditions are right for a latching current to be established within the period of the gate pulse.

When switching on an inductive load the initial current will increase from zero at a rate dependent on the voltage across and the inductance of the load (the minimum voltage being determined by the load current detector). To help with latching, additional triac load current for a short duration can be provided if required by means of a series RC network in parallel with the triac. C_1 and R_{10} provide this function as well as offering some protection from dv/dt triggering of the triac due to noise spikes on the mains.

OVERLOAD CURRENT PROTECTION

The purpose of motor current limitation is more to protect the triac than the motor itself. Since the stall current is generally much higher than that required for maximum working torque, a limitation can be set at a lower value thus guaranteeing safe operation of the triac under all load conditions.

Peak load current limiting can be provided by discharging the ramp generator capacitor (pin 7) with a current that is proportional to the current drawn from pin 3, when the trip threshold is exceeded. This reduces the internal speed reference voltage (V_s) to a level such that a reduction in phase angle conduction is made, hence reducing the load current. The current limit input is a common base transistor which conducts when the emitter, connected to pin 3, is driven negatively with respect to common (pin 8). The current gain (A_{fl}) is the ratio of the discharge current from pin 7 to the current drawn from pin 3.

Load current is monitored by means of a low value resistor (R_{11}) connected in series with the load. The voltage developed across this resistor drives the current limit circuit via resistors R_3 and R_8, such that the voltage on pin 3 is zero at the desired peak load current. The sensitivity of the circuit (i.e. the rate at which the circuit reacts to over-current) will depend on the drive impedance, this being predominantly determined by the resistance of R_8. With a circuit as shown in the reference circuit diagram the load current is monitored in the negative supply cycle.

The value of R_{11} is normally chosen such that a fraction of a volt is generated across it, thus minimising power dissipation yet providing a reasonable signal to drive the overload current circuit. The peak load current is determined by

$$I_{pl} = \frac{V_{cc}}{R_{11}} \times \frac{R_8}{R_3} \text{ A} \quad \ldots 20$$

High frequency noise may be generated by short duration changes in load current produced by commutator action in a motor load. Due to the low impedance required R_{11} will normally be a wire wound resistor and hence have some inductance, which will increase the noise voltage driving into pin 3. This can be filtered by the inclusion of capacitor C_4.

If overload current limiting is not required, pin 3 should be left open circuit.

CURRENT CONSUMPTION

The total supply current required can be calculated from the sum of the following:

I IC operating current

This is the current required by the circuit which is not dependent on external circuitry.

$$i_I = 7.4\text{mA} \pm 20\% \quad \ldots 21$$

II Slow ramp generator current

This is usually very small and may be neglected. If required it may be calculated from:-

$$i_{II} = \frac{V_{CC}}{R_{20}} \times 10^3 \text{ mA} \quad \ldots 22$$

III Frequency to analog conversion current

This is the additional dynamic operating current required. Again this is usually negligible but may be calculated from:-

$$i_{III} = f_t (V_{cc} - 2V_{be}) C_{11} (1 + A_I) \times 10^3 \text{ mA} \quad \ldots 23$$

IV Voltage and current synchronisation currents

The AC input currents to pins 1 & 2 cause a drain from the positive sypply, the additional current required is given by:-

$$i_{IV} = \frac{\sqrt{2}\, V_{AC}}{\pi} \left(\frac{1}{R_4} + \frac{1}{R_5} \right) 10^3 \text{ mA} \quad \ldots 24$$

V Pulse timing current

This is the dynamic operating current of the pulse timing circuit which is determined by the current fed into pin 15. Normally this current is small and has little effect on the total current required.

$$i_V = \frac{2(V_{cc} - V_{be})}{R_{21}} \times 10^3 \text{ mA} \quad \ldots 25$$

VI Triac gate current

The average triac gate drive current may be calculated from

$$i_{VI} = 2f_m \times t_p \times I_{tg} (1 + P_t) \times 10^{-6} \text{ mA} \quad \ldots 26$$

The probability factor P_t has been incorporated to take account of current required for additional triac pulses. These will only be required if the load current is interrupted, for example by motor brush bounce.

VII Other external circuitry

Regulated supply current may also be required for biasing control inputs to pins 5 and 7 and other auxilliary circuitry.

When a reset condition exists the IC operating current increases by a maximum of 1mA. This will occur when the supply is being established hence this current needs to be catered for. However during a reset condition no triac pulses will be generated, therefore only the greater of these two currents needs to be provided.

When calculating the supply current required, the worst case conditions (i.e. component tolerance etc) should be incorporated in the above equations.

$$I_s = \Sigma i \qquad \ldots 27$$

VOLTAGE REGULATOR CIRCUIT

A shunt type voltage regulator circuit is incorporated in the circuit to maintain a steady positive supply on pin 9. This enables the device to be driven direct from the mains via current limiting and smoothing components. Since the current shunt (pin 10) is not directly connected to the positive supply (pin 9) it is also possible to power the circuit direct from a DC supply or use pin 10 to drive a series regulating transistor as shown in Fig.2.

A voltage monitor circuit senses the voltage on pin 9 (V_{cc}), this inhibits triac firing pulses and resets the timing functions until an adequate supply for correct circuit operation has been established. Hysteresis in the monitor circuit gives rise to two trip levels, namely the enable (V_{me}) and disable (V_{md}) voltages.

Where use is made of the shunt regulator, unwanted current is drained by pin 10 to common. Power dissipation by the device can be minimised by incorporating resistor R_{22}, enabling greater supply currents to be regulated. Under worst case conditions it is important that the voltage dropped across this resistor does not exceed 13volts.

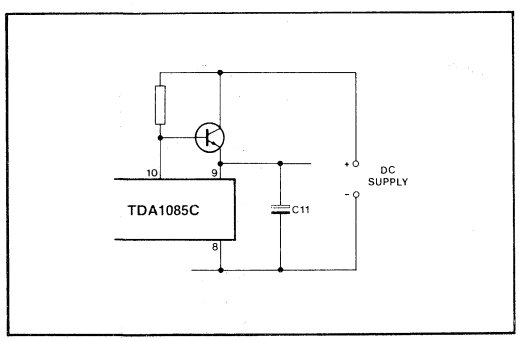


Fig.2 Series regulated DC supply

AC SUPPLY CIRCUITS

The simplest AC supply circuit is shown in Fig.3. This circuit will produce ripple on the regulated supply (pin 9) and will hence cause some asymmetry in firing between positive and negative cycles of the mains. Component values may be calculated from:

$$C_{11} = \frac{I_s}{V_{cr} \times f_m} \times 10^3\ \mu F \qquad \ldots 28$$

$$R_1 = \frac{\frac{\sqrt{2}}{\pi} V_{ac} - V_{cc}}{I_s\,(mA)} \times 10^3 \text{ ohms} \qquad \ldots 29$$

$$P_{dr} = \frac{(\sqrt{2}\,V_{ac} - V_{cc})^2}{4R_1} \text{ Watts} \qquad \ldots 30$$

Where it is important to provide symmetrical firing, further filtering of the AC supply will be required as shown in Fig. 9. Although additional components are required the total capacitance is less than that required in the simple circuit.

The circuit should be designed such that the half wave rectified current is roughly smoothed by capacitor C_2. R_2 and C_2 are chosen such that they are capable of maintaining the average current required by the circuit (I_s).

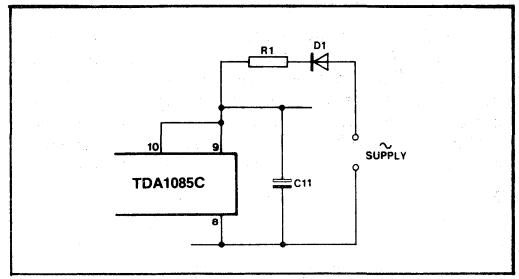


Fig.3 Simple shunt regulated supply

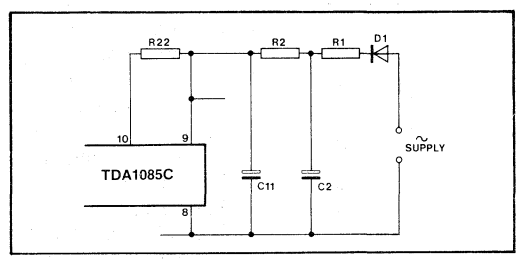


Fig.4 Resistive feed shunt regulated to provide a low ripple supply

The peak demands during triac gate pulses are then catered for by capacitor C_{11}. The dropper resistors may be calculated from:

$$R_1 + R_2 = \frac{\frac{\sqrt{2}}{\pi} V_{ac} - V_{cc}}{I_s(mA)} \times 10^3 \text{ ohms} \qquad \ldots 31$$

$$P_{dr} = \frac{(\sqrt{2}V_{ac} - V_{cc} - I_s R_2)^2}{4R_1} \text{Watts} \qquad \ldots 32$$

Where power dissipation is a problem the circuit may be powered by a reactive feed from the AC supply as shown in Fig.3. Resistor R_x should be included to limit current due to noise spikes from the supply. An impedance of the order of 200 ohms is suitable for this purpose. Neglecting the effects of this resistor, the value of capacitor C_x may be calculated from:

$$C_x = \frac{I_s}{f_m\,(2\sqrt{2}V_{ac} - I_s R_2 - V_{cc})} \times 10^3 \mu F \qquad \ldots 33$$

NB *Worst case conditions should be put in the above equations when calculating component values etc.*

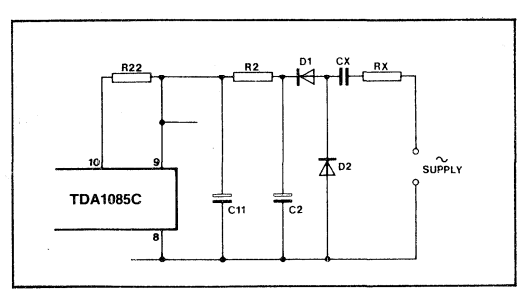


Fig.5 Reactive feed shunt regulated to provide a low ripple supply with minimum power dissipation

TRIAC LATCHING CIRCUIT

When driving inductive loads a series RC network may be required across the triac. This is to provide a short duration load current in the triac while the current in the main inductive load is being established after a gate pulse is applied. In this way a latching current can be quickly established, even when the triac is fired at low voltage points in the mains cycle. C_1 and R_{10} provide this function as shown in Fig.1.

SYMBOLS USED IN TEXT

Symbol	Function	Units
A_{il}	Current limit gain	—
A_t	IC tacho conversion gain	—
f_m	Mains frequency	Hz
f_f	Tacho frequency	Hz
I_d	Pulse ramp discharge current	μA
I_r	Pulse ramp recharge current	μA
I_{rf}	Fast ramp current	mA
I_s	Supply current	mA
I_{tg}	Peak triac gate current	mA
K	Tacho conversion factor	mV/Hz
N	Number of tacho poles	—
P_{dr}	Power dissipation by dropper resistor (R1)	Watts
P_t	Probability of extra triac pulse	—
S	Motor speed	RPM
t_d	Distribution period	seconds
t_p	Pulse duration	μs
t_r	Pulse retriggering rate	μs
V_{ac}	AC supply voltage (RMS)	volts
V_{be}	Transistor emitter base voltage	volts
V_{cc}	Positive rail voltage (pin 9)	volts
V_{cr}	Supply ripple voltage	volts
V_f	Analog feedback voltage	volts
V_{fr}	Feedback voltage ripple (pk—pk)	mV
V_{me}	Voltage monitor enable level	volts
V_{md}	Voltage monitor disable level	volts
V_p	Phase control voltage	volts
V_{ra}	Ramp voltage at first knee	volts
V_{rb}	Ramp voltage at second knee	volts
V_{rf}	Fast ramp rate	mV/s
V_{rp}	Dynamic ramp voltage	volts
V_{rs}	Slow ramp rate	mV/s
V_s	Internal speed reference voltage	volts
V_{tg}	Triac gate voltage	volts
V_{fo}	Tacho offset voltage	mV
V_{fx}	Voltage across triac	volts
V_5	Speed program voltage on pin 5	volts
V_6	Distribution level programmed on pin 6	volts
V_{13}	Pulse drive voltage from pin 13	volts

Table 1

THE UNIVERSAL MOTOR

This is a machine which has a commutator drive to the armature and a field that is polarised by the supply. The field and armature may be series or parallel connected such that the machine in principle could be driven from a DC or AC supply. Most domestic type motors are series connected.

In controlling this type of machine, the phase angle may be varied from zero to a maximum determined by the lag in load current due to inductance. To obtain full power it is therefore necessary to have a load current detection circuit such that the triac is not fired before the current from the previous half cycle has reduced to zero.

At high motor speeds brush bounce may also be a problem. This can cause an interruption in load current and hence unlatch the triac, reducing the power to the motor. To overcome this problem it is necessary to detect the situation and retrigger the triac.

Both these problems are overcome in the TDA1085C circuit by means of the load current synchronisation circuit (pin 1).

THE FIXED FIELD MOTOR

This is a machine which has a constant field which may be provided by permanent magnets in the stator. The armature requires a DC supply to drive the motor, and hence this may be said to be a DC machine.

This type of motor may be driven from an AC supply by means of a rectifying circuit. The machine will generate a back EMF that is proportional to its speed and will therefore only draw load current when the supply voltage is greater than the generated EMF.

When driving this type of load with a phase control circuit the triac cannot be latched before a 90° phase angle since the EMF generated will be almost equal to the peak supply voltage from previous cycles, and hence no load current will flow until the peak supply voltage is reached again. For this reason it is desirable to be able to limit the triac gate pulse to the second half of each half cycle of the supply. With the TDA1085C the maximum conduction angle may be limited by restricting the voltage on pin 16 by means of a zener diode.

Since load current only follows for a short period of each half cycle a high peak current is to be expected. This, if unchecked, may cause damage to the triac and rectifying devices. By incorporating an inductor in series with the motor, the load current may be controlled in its build-up rate and spread over a greater period, hence reducing its peak value for a particular load demand.

THE INDUCTION MOTOR

The principle of an induction motor is to generate a rotating magnetic field in which the rotor is placed. Due to the generation of eddy currents the rotor will react and follow the field. The difference between the field and rotor speeds is known as the slip speed which increases with applied load.

The main disadvantage of this type of machine is that it has a poor torque speed characteristic which makes it unsuitable for variable speed applications where a high torque is required at low speeds. They may however, be suitable for driving loads such as fans or centrifugal pumps where the load torque reduces with decreasing speed.

Due to the high inductance of this type of machine a poor load power factor results. This may be improved by running the motor at a fixed slip speed by the use of a phase control circuit. A significant saving in real power consumed will also be obtained when the motor is lightly loaded.

When using phase control with this type of motor it is most important that symmetrical firing of the positive and negative waves is achieved otherwise a small net DC voltage may generate a high DC current in the stator windings. The TDA1085A is capable of meeting this requirement.

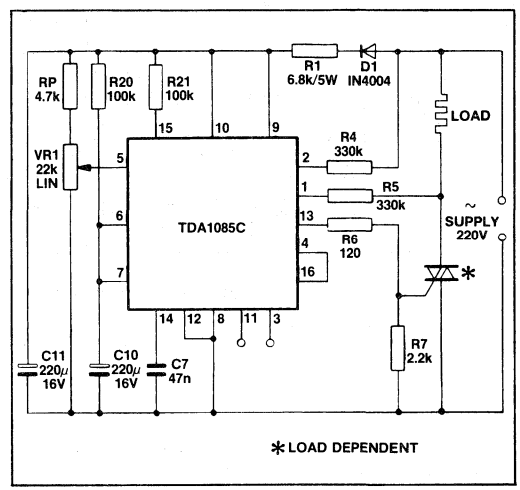


Fig.6 Manual phase control circuit

MANUAL PHASE CONTROL CIRCUIT

Fig.6 shows an open loop phase control circuit using the ramp generator of the TDA1085C to limit the rate of increase of the phase angle. R_{20} and C_{10} give a time constant of 22 seconds.

UNIVERSAL MOTOR APPLICATION

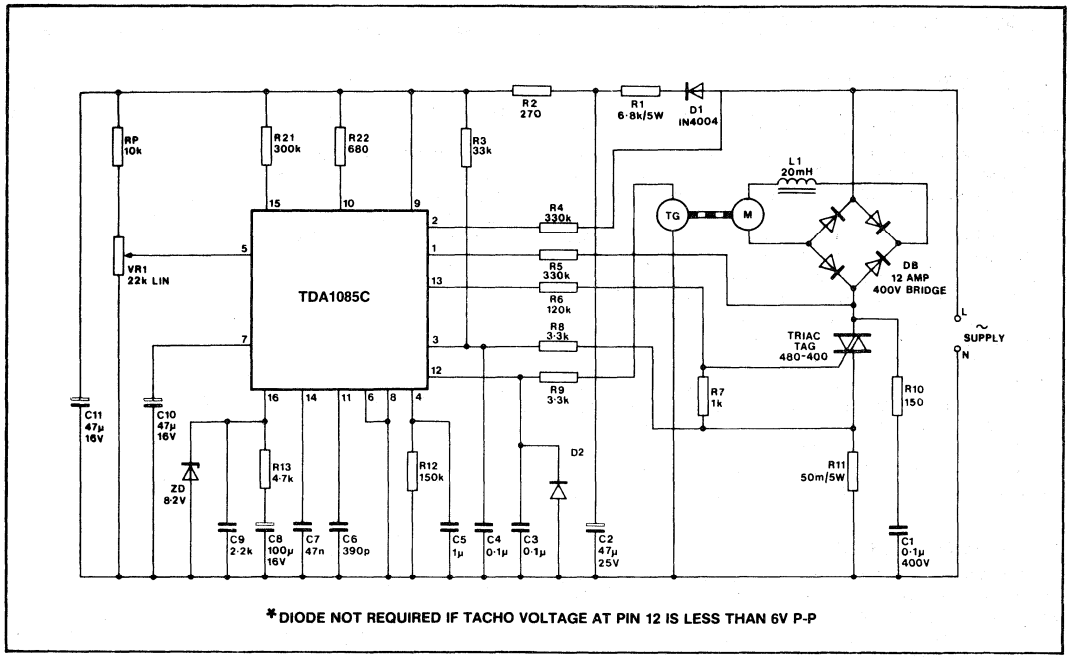
The circuit of Fig.6 is essentially the same as the reference circuit Fig.1, but with component values added. The specification is as follows:

Supply:	220V ± 15% 58Hz
Motor:	Normal load current 7A RMS
	Peak load current limit 21A
Tacho:	8 poles
	Amplitude at max. speed 14V RMS
Motor speed requirements	Wash speed 800RPM
	Distribute speeds 600 to 1200RPM
	Spin speeds 5,000RPM
	Super spin speeds 10,000RPM
Distribution time:	20 seconds

FIXED FIELD MOTOR APPLICATION CIRCUIT

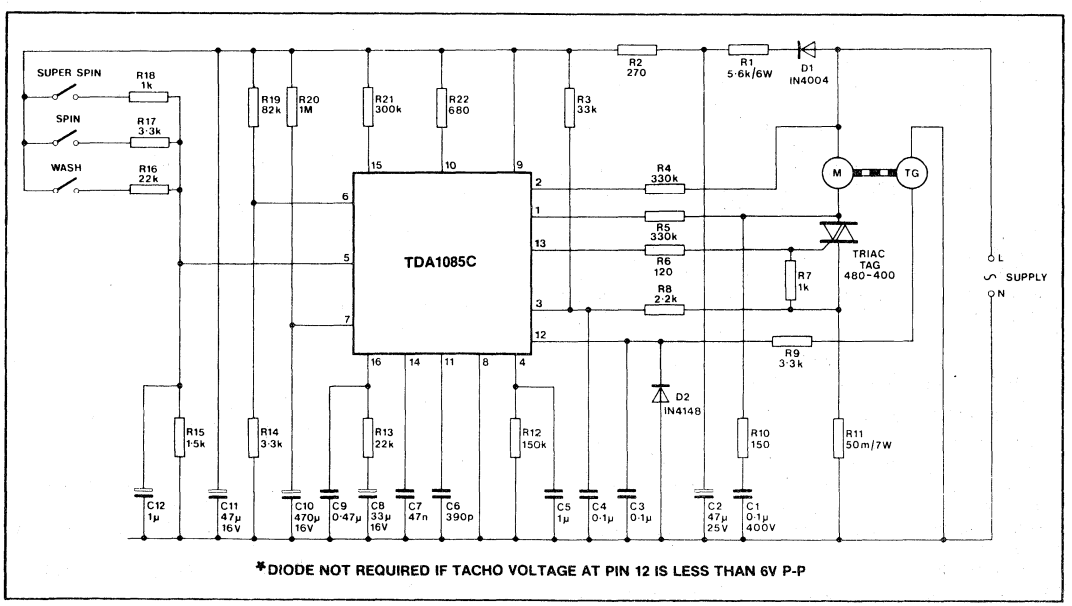
Specification for the circuit shown in Fig.7:

Supply:	220V ± 15% 50Hz
Motor:	Peak load current limit 30A
Tacho:	8 poles
	Amplitude at maximum speed 14V RMS
Motor speed:	Variable up to 10,000 RPM



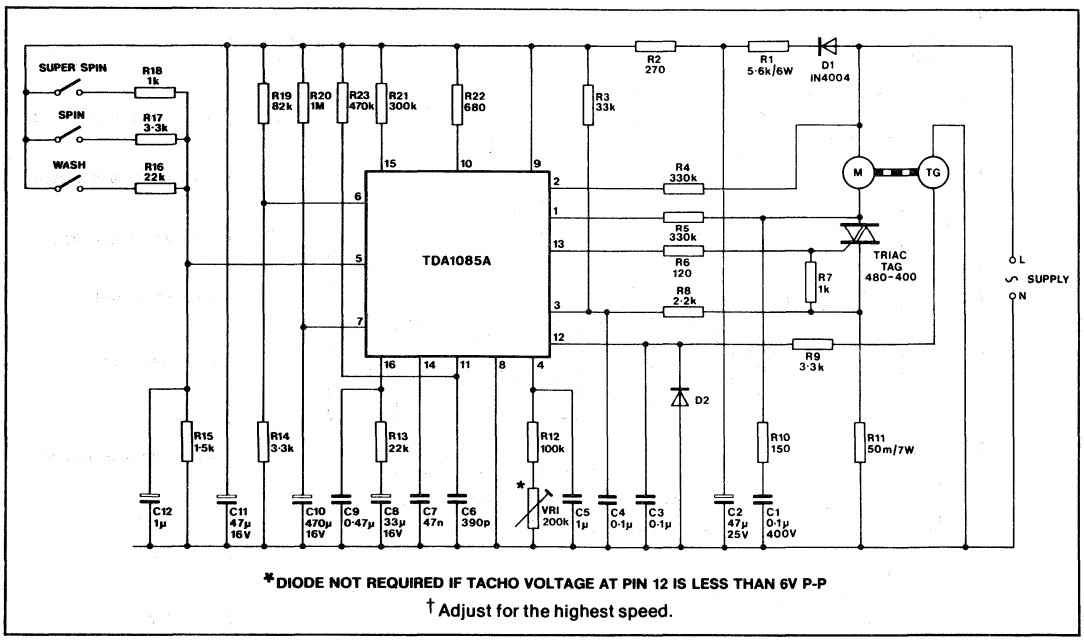
*DIODE NOT REQUIRED IF TACHO VOLTAGE AT PIN 12 IS LESS THAN 6V P-P

Fig.7 Fixed field motor application circuit



*DIODE NOT REQUIRED IF TACHO VOLTAGE AT PIN 12 IS LESS THAN 6V P-P

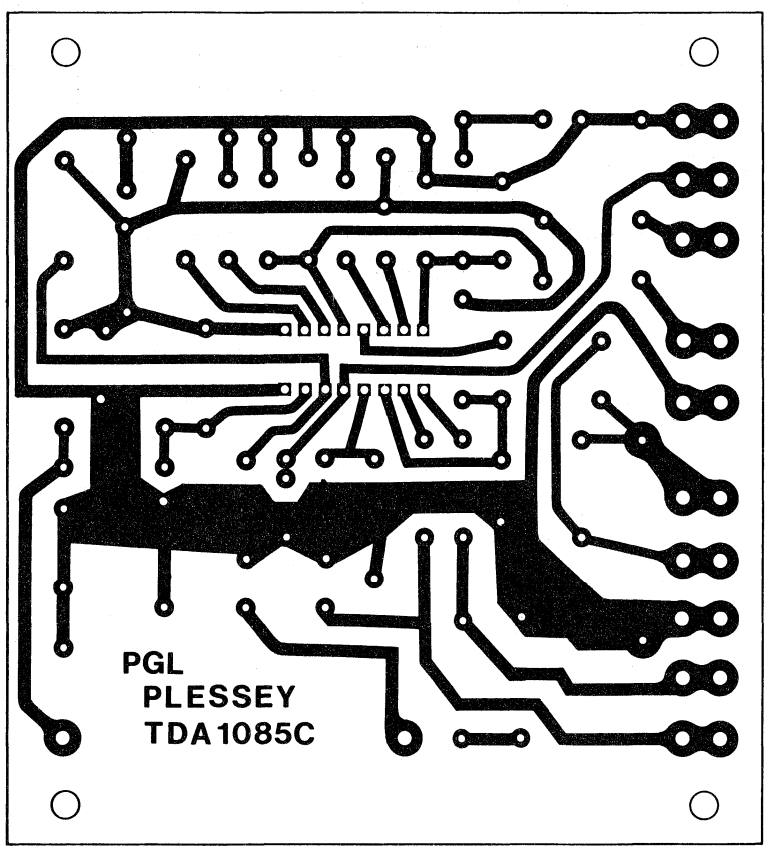
Fig.8 Universal motor application circuit



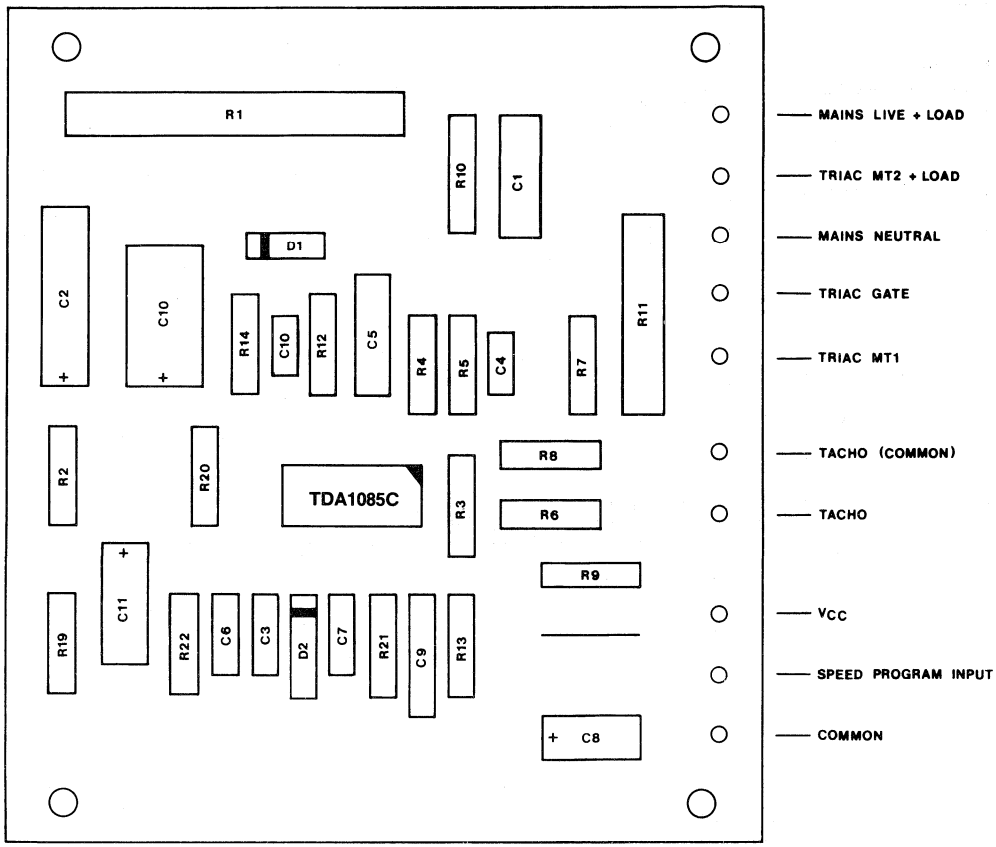
*DIODE NOT REQUIRED IF TACHO VOLTAGE AT PIN 12 IS LESS THAN 6V P-P

† Adjust for the highest speed.

Fig.9 Calibrated universal motor application circuit



(a) Copper side



(b) Component layout

*** DIODE NOT REQUIRED IF TACHO VOLTAGE AT PIN 12 IS LESS THAN 6V P-P**

Fig.10 PCB for motor speed control applications

System Design with the TDA2086A

Throughout this section, component references are those shown on the Reference System Circuit Diagram, Fig.2. See Table 1 for Symbol Definitions.

OPEN LOOP OPERATION

The simplest method of motor speed control using electronics is an open loop system. In an open loop system, the phase angle of the triac firing pulse is determined by the program input voltage on pin 10. The TDA2086 is particularly useful in open loop applications due to the well-defined control voltage/phase angle relationship. In this mode, changes in motor loading will cause corresponding variations in motor speed but regulation will be a considerable improvement over that achieved when motor speed regulation is obtained by conventional series dropper resistor.

CLOSED LOOP CONTROL

A block diagram of a basic closed loop speed control system is shown in Fig.1. In this case, a voltage proportional to motor speed is compared by the amplifier with the speed program voltage and any difference will cause an appropriate change in firing pulse angle and hence motor speed. In this way automatic compensation for changing motor loads can be made.

In addition to the basic speed control functions mentioned above, additional circuitry is provided to allow control of motor acceleration and reduction of firing pulse phase angle in case of motor overload.

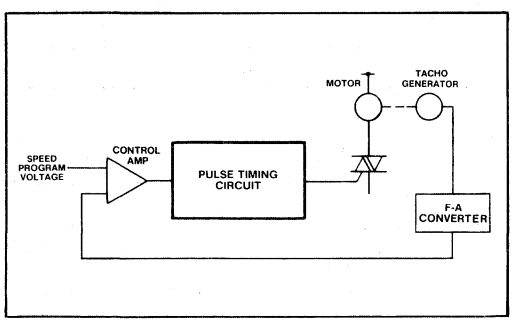


Fig.1 Basic closed loop control system

FEEDBACK VOLTAGE

An analog feedback voltage of 0V to -5V, obtained by rectifying and smoothing the output from a tacho generator, may be applied to pin 13. If analog feedback is used, the frequency to analog converter circuitry must be made inoperative by connecting pin 15 to ground and leaving pin 14 open circuit.

In most motor control applications digital feedback is recommended as this method has the advantage of inherent stability against tacho ageing and temperature drift whilst requiring no speed calibration.

Direct connection of the tacho is possible with perhaps a small capacitor to ground to reject noise, as signal amplitude is unimportant; provided the minimum value is greater than about 350mV peak which is necessary to overcome hysteresis plus input offset voltage.

An open circuit tacho will allow the tacho input to be pulled negative by the bias current until a general reset is initiated at a trip level of about -5.5V. In order to prevent a reset condition during normal operation it is necessary to limit the tacho signal to a value significantly less than the trip level, this being achieved by the capacitor C10 and resistor R6, which are chosen to give a substantially constant input voltage at all speeds.

Frequency to Analog Converter

The frequency to analog converter is used with digital feedback to convert the frequency of the tacho input to an analog voltage suitable for application to the control amplifier.

During negative half cycles at the tacho input, C4 is charged by an internally generated current of nominally 100μA until -5.5V is reached, at which point the capacitor is rapidly discharged. Each time C4 is charged a pulse of current equal to and designed to track with that at pin 14 is integrated at pin 13 by C6, producing a DC voltage proportional to motor speed.

By choosing a suitable conversion factor for the frequency to analog converter it is possible to design a system to run at any given speed within the 0V to -5V control voltage range at pin 10.

Example: A motor fitted with an 8 pole tacho is required to run at 5000 rev/min with a control voltage at pin 10 of 2.5V. Calculate the values of C4 and R3 required.

Since at steady speed the control voltage at pin 10 and the F-A output voltage at pin 13 must balance, C4 and R3 must be chosen to give 2.5V at pin 13 at a motor speed of 5000 rev/min.

The analog feedback voltage (Vf) generated by the converter circuit is given by

$$Vf = Kft \times 10^{-3} \text{ Volts} \quad ...1$$

where K is the conversion factor given by

$$K = \frac{C4 \quad R3}{200} \text{ mV/Hz} \quad ...2$$

and ft is the tacho frequency given by

$$ft = \frac{SN}{120} \text{ Hz} \quad ...3$$

using 1 and 3 above

$$K = \frac{2.5V}{0.333} = 7.5\text{mV/Hz}$$

choosing R3 = 150kΩ in the range 100kΩ to 470kΩ and using 2 above

$$C4 = \frac{7.5 \times 200}{150k} = 10\text{nF}$$

Provided close tolerance components are used for C4 and R3, most systems should not need calibration, but if required R3 can be replaced by a series resistor/potentiometer combination to give precise speed adjustment.

The value of capacitor C6 on pin 13 is a compromise between F-A converter response time and ripple voltage at the control amplifier input. In most systems a value of 1μF will be sufficient.

Under some conditions noise introduced into the tacho coil by vibration of the stationary motor armature when power is first applied, or by electromagnetic induction can produce sufficient feedback to prevent motor start up, the

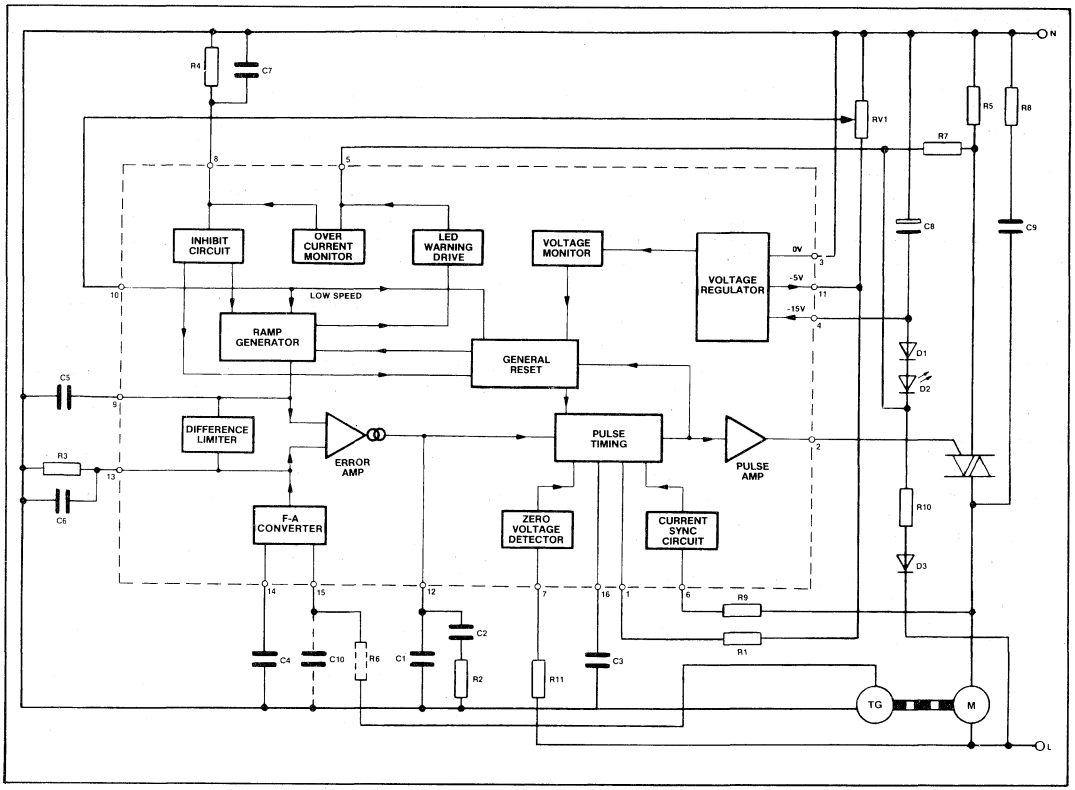


Fig.2 Reference system circuit diagram

phase control system using the tacho noise as evidence that the motor is running. This condition is most likely with the TDA2085A where the tacho is connected directly to pin 15 without a capacitor to ground. A cure can usually be found by connecting a capacitor to ground or in difficult cases a series resistor as well.

RAMP GENERATOR

The ramp generator limits the rate of change of speed reference voltage (Vs) applied to the control amplifier and therefore controls the rate of acceleration of the motor. The ramp rate Vr is set by an internally generated 30μA current source Ir and the capacitor C5 on pin 9, the rate being given by

$$Vr = \frac{Ir \times 10^{-6}}{C10} \text{ V/s} \qquad ...4$$

Using the previous example where the control voltage is increased from zero to -2.5V and with C5 = 10μF the ramp rate (Vr) will be

$$\frac{30 \times 10^{-6}}{10 \times 10^{-6}} = 3.0\text{V/s}$$

and the acceleration time $= \frac{2.5\text{V}}{3.0\text{V/s}} = 0.83$ seconds

The final ramp voltage on pin 9 is 2Vbe below the control voltage on pin 10.

SPEED PROGRAM VOLTAGE

The speed program voltage (V10) on pin 10 has a working range from the zero power demand level at -75mV and Vreg. Levels above 75mV on pin 10 will cause the ramp capacitor to remain discharged and the triac drive pulse will be inhibited. The LED on pin 5 will also remain lit.

In most applications pin 10 voltage will be derived from a potentiometer connected between Vreg and ground.

THE CONTROL AMPLIFIER

In closed loop applications, the control amplifier is used to compare the analog feedback voltage (Vf) at pin 13 with the speed reference voltage on pin 10 and to produce a phase control voltage Vp on pin 12. The amplifier has a transconductance gain of 100μA/V with a limited bidirectional output drive capability of $\pm$25μA. Proportional control therefore occurs for differential input errors between $\pm$250mV.

The gain and phase compensation for closed loop control systems are determined by C1, C2 and R2 on pin 12. These components are best chosen empirically to achieve a compromise in terms of speed overshoot.

For open loop control, the control amplifier may be used as a buffer by connecting pin 12 to pin 13 and disabling the F-A converter by grounding pin 15. Use may still be made of the ramp generator to control the maximum rate of phase angle increase.

If required the maximum phase angle can be controlled by a clamp voltage applied to pin 12 but care must be taken to ensure a sharp turn-on knee.

ZERO VOLTAGE DETECTOR

The zero voltage detector resets the pulse timing circuit ramp generator at the zero points of each mains cycle. The mains voltage is applied via a high value current limiting resistor R11 to pin 7 and a reset pulse is generated whenever the input current is between $\pm 50\mu A$.

The circuit is designed to give symmetrical switching about the zero voltage points ensuring symmetrical triac firing in positive and negative mains half cycles.

The value of R11 should be chosen to limit the peak current in pin 7 to less than $\pm 1mA$.

CURRENT SYNC CIRCUIT

The current sync circuit operates in conjunction with the pulse timing circuit by supplying an enable signal dependent on the conduction state of the triac. The enable signal is generated if the voltage across the triac is sufficient to produce an input current to pin 6 via R9 greater than $\pm 50\mu A$.

Peak current to pin 6 should be limited to below $\pm 1mA$.

PULSE TIMING CIRCUIT

The function of the pulse timing circuit is to control the delay and duration of the triac firing pulse. A ramp voltage is produced on the pulse timing capacitor C3 on pin 16 which is charged by a constant current determined by R1 on pin 1. The ramp is reset by the voltage sync circuit at each mains zero crossing. A triac firing pulse is produced when the ramp voltage reaches a level determined by the control amplifier output on pin 12 unless further delayed by the current sync input pin 6.

Full power may be supplied to inductive loads since, when maximum conduction is demanded, the triac pulse is delayed until the lagging load current from the previous half cycle has reduced to zero. At this point the triac will cease to conduct and the supply voltage will appear across it, which when detected by the current sync input, initiates the next triac pulse.

At high motor speeds brush bounce may become severe, causing interruptions in motor supply current and unlatching of the triac. Under these conditions the current sync circuit will initiate a retriggering pulse to the triac.

The ramp waveform is generated by rapidly charging C3 on pin 16 to a Vbe more negative than Vreg at the mains zero voltage crossing. After the zero voltage point, C3 is discharged in a linear fashion by a current (Id) defined externally on pin 1 by R1. When the voltage on C3 reaches a value determined by the control amplifier on pin 12 a triac gate pulse is initiated. The dynamic working range of the ramp generator is approximately equal to Vreg.

The triac pulse duration is determined by recharging C3 to nominally 50mV above the original trip voltage.

If retriggering occurs the delay will be determined by the time taken for the current Id to discharge C3 back to the original trip voltage.

Triac Pulse Timing Equations

Ramp discharge current

$$Id = \frac{(Vreg - Vbe)}{R1} \times 10^6 \mu A \qquad ...5$$

Dynamic ramp voltage on pin 16

$$Vrp = \frac{Id \times 10^{-6}}{2 \times fm \times C3} V \qquad ...6$$

For full phase control the calculated value of Vrp must be less than Vreg.

In most applications standard values can be used for C3 and R1. These are:

For 50Hz supply

C3 = 47nF ± 10%

R1 = 200kΩ ± 5%

For 60Hz supply

C3 = 47nF ± 10%

R1 = 160kΩ ± 5%

With the above components the triac pulse width will be approximately $70\mu s$ and the retriggering time $100\mu s$.

TRIAC GATE DRIVE

The triac gate pulse is negative going, this being preferred by triac manufacturers and in most cases it will be found that the triggering current requirement is less for negative pulses. Internal current limiting is provided, the current being largely independent of the triac gate voltage although a series resistor can be used to reduce overall power consumption if required.

When a series resistor is used the approximate gate drive current may be calculated from

$$Itg = \frac{V4 - 1 - Vtg}{Rg} \times 10^3 mA \qquad ...7$$

provided the series resistor is sufficient to reduce the gate current below the internally limited value.

TRIAC LATCHING

As mentioned before, it is necessary to trigger the triac when conditions are right for a latching current to be established within the period of the gate pulse.

When switching on an inductive load the initial current will increase from zero at a rate dependent on the voltage across and the inductance of the load (the minimum voltage being determined by the load current detector). To help with latching, additional triac load current for a short duration can be provided if required by means of a series RC network in parallel with the triac. C9 and R8 provide this function as well as offering some protection from dv/dt triggering of the triac due to noise spikes on the mains.

LOAD CURRENT LIMITING

The purpose of motor current limitation is more to protect the triac than the motor itself. Since the stall current is generally much higher than that required for maximum working torque, a limitation can be set at a lower value thus guaranteeing safe operation of the triac under all load conditions.

The load current is normally sensed in the positive mains half cycle by means of a low value resistor R5 in series with the triac and load. This voltage drop is converted back into a low current source by R7 in series with pin 5 and is mirrored internally with a ratio of 2:1 into pin 8. Peak current limiting can be provided at this point by inserting a resistor between pin 8 and common whereas average current limiting requires the addition of an integrating capacitor.

When average current limiting is used the double action of the inhibit circuits on pin 8 is utilised. This has two trip points at -1V (load current limit) and -1.5V (load current inhibit). When the first trip point (-1V) is reached the power to the load will be gradually reduced by decreasing the voltage on the ramp capacitor, (the discharge rate being equal but

opposite to the soft start), hence reducing the power and providing a constant current drive (producing constant torque) to the motor. When the second trip point (-1.5V) is reached a general reset of all timing functions occurs at a fast rate, hence if a gross overload was suddenly applied to the motor, a rapid reduction in power supplied would result. Since it is not possible to turn the triac off during a cycle, the triac and motor should be chosen to be capable of withstanding one complete mains cycle under the worst overload condition.

The value of R5 can be calculated from

For load current limit

$$\frac{\frac{1}{R4} \times R7}{\text{Average load current} \times 0.25} \quad ...8$$

For load current inhibit

$$\frac{\frac{1.5}{R4} \times R7}{\text{Average load current} \times 0.25} \quad ...9$$

The value of R4 can vary between 100kΩ and 470kΩ, the lower value being preferred in order to reduce offset voltages produced by pin 8 bias current. When the LED drive capability of pin 5 is used the overload current level will be increased by about 20%.

In high current applications where the power dissipated in a series sensing resistor would be unacceptable, a current transformer may be used as shown in Fig.3.

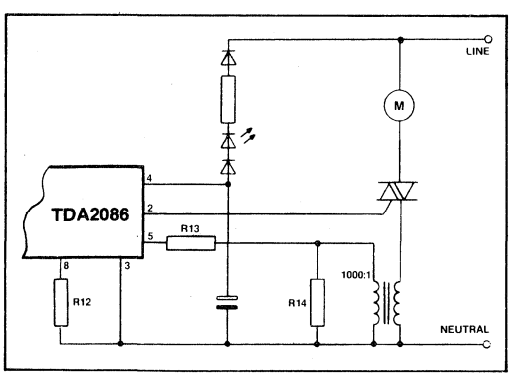


Fig.3 Current transformer application

With a 1000:1 current transformer the average overload current can be calculated from

For load current limit

$$\frac{4 \times 1000 \times R13}{R14 \times R12} \quad ...10$$

For load current inhibit

$$\frac{4 \times 1.5 \times 1000 \times R13}{R14 \times R12} \quad ...11$$

Suitable values for R12 and R13 are 100kΩ and 5.6kΩ.

Peak load current limiting tends to produce a foldback action (of motor speed and torque) at large conduction phase angles. This is due to the peak current initially increasing when the phase conduction angle is reduced at constant load torque. If peak current limiting is adequate, capacitor C7 can be removed and the peak overload current calculated from

$$\frac{R7 \times 1.5}{R5 \times R4 \times 0.5} \quad ...12$$

INHIBIT CIRCUIT

As previously stated the inhibit circuit has two trip levels normally used in load current limiting but if required a general reset can be initiated by the application of a voltage between -1.5 and -Vreg to pin 8. This feature allows on/off control by external control circuitry or the fitting of a PTC thermistor to sense motor winding temperature as shown in Fig.4. At normal temperatures pin 8 is held close to the 0V rail as the thermistor resistance is low, but as the thermistor critical temperature is approached, the resistance increases rapidly until pin 8 voltage falls below -1.5V when the power to the load is removed.

LED DRIVE CIRCUIT

The LED drive circuit is designed to drive an LED in series with the device such that the IC supply current is used to drive the LED thereby minimising overall power consumption.

In order to turn the LED off an internal circuit with a voltage drop lower than the LED plus its associated silicon diode is used to shunt current from the LED.

Due to the multiplexing technique used on pin 5 whereby IC supply current is provided during negative half cycles and load current monitoring during positive half cycles some additional current, usually amounting to about 0.5mA will be required when the LED drive facility is used.

Due to SCR latching associated with the LED drive circuit it is not possible to use the LED feature with or without load current limiting if the circuit is powered from DC supplies.

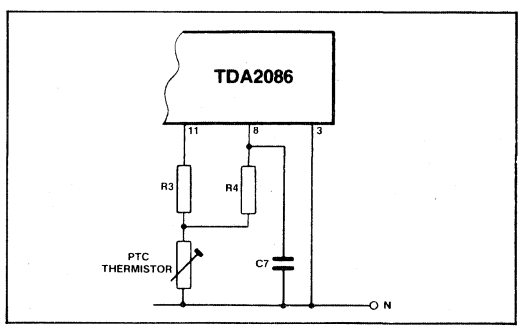


Fig.4 Over-temperature shut-down

AC SUPPLY CIRCUITS

The TDA2086 circuit has been designed for very low power consumption, this parameter being particularly important when operating from mains voltages via a dropper resistor.

When calculating the value of dropper resistor required additional currents such as those required by the control potentiometer on pin 10 or any other ancillary circuitry powered from the -5V or -15V supplies must be added to the IC supply current.

The circuit design whereby all critical control circuitry is powered from a -5V series stabilised supply ensures that the circuit is insensitive to ripple on the -15V line, thus enabling a single dropper resistor and capacitor to be used as shown in Fig.5.

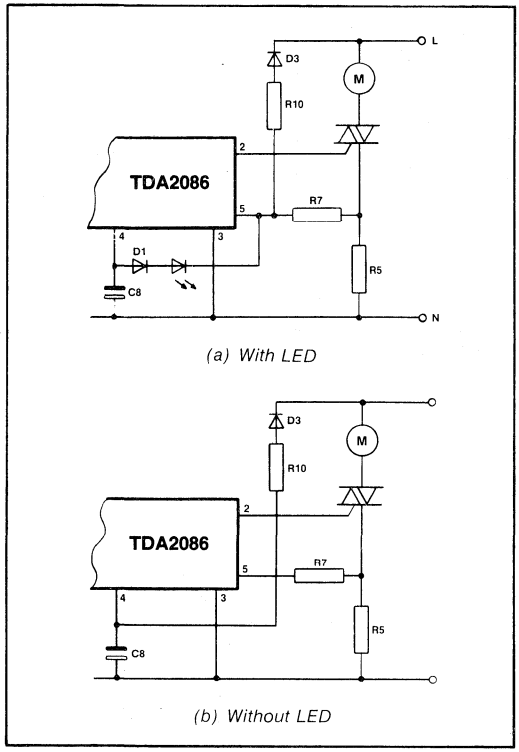


Fig.5 Mains supply circuit

Component values can be calculated from

$$C8 = \frac{Is}{Vcr \times fm} \times 10^3 \mu F \qquad ...13$$

$$R10 = \frac{\frac{\sqrt{2}}{\pi} Vac - Vcc}{Is\ (mA)} \times 10^3 \Omega \qquad ...14$$

$$Pdr = \frac{(\sqrt{2}\ Vac - Vcc)^2}{4R10}\ W \qquad ...15$$

The low current requirement of the TDA2086 reduces the power dissipation in the mains dropper resistor to below 2W, but in some cases even this level of power can be undesirable. By using a reactive feed arrangement the power loss in the dropper resistor is eliminated, but due to the phase shift introduced by the reactive feed capacitor, the multiplexing of current overload and LED drive on pin 5 will not function.

Figure 6a shows a reactive feed using the LED drive feature, and Fig.6b reactive feed with current overload.

The value of Cx can be calculated from

$$Cx = \frac{Is\ (mA)}{fm\ (2\sqrt{2}\ Vac - Vcc)} \times 10^3 \mu F \qquad ...16$$

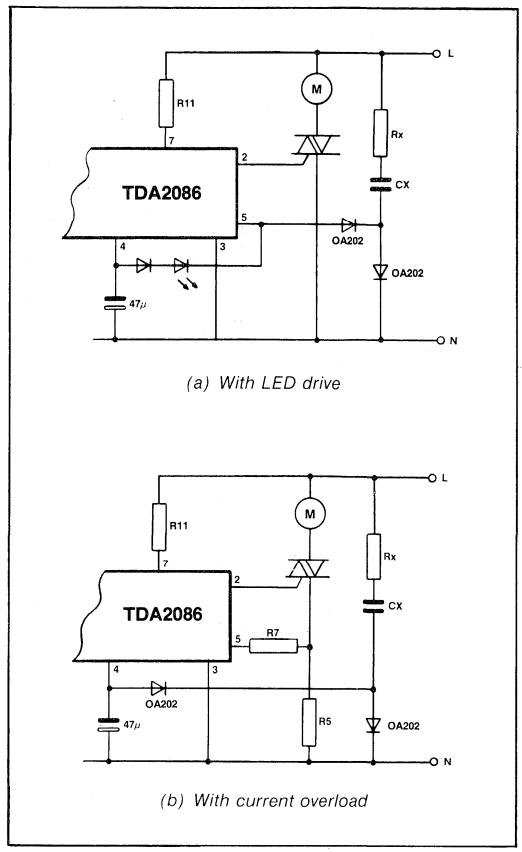


Fig.6 Reactive feed circuits

Resistor Rx is included to limit current due to noise spikes on the supply, a value of 330Ω being suitable.

OPERATION FROM DC SUPPLIES

Operation from stabilised or unstabilised DC supplies is possible provided a signal in phase with the mains is available to drive the voltage sync input on pin 7.

If a stabilised supply is used, the voltage must always be set between the maximum shunt stabiliser voltage on pin 4 and the minimum voltage monitor enable level. Supplies outside these limits will prevent circuit operation or cause damage to the chip through excess power dissipation.

When operation from an unstabilised DC supply is required, the circuit shown in Fig.6 should be used. R1 value being calculated from

$$\frac{Vss - Vcc}{Is\ (mA)} \times 10^3 \Omega \qquad ...17$$

To ensure a relatively constant current through R1 the unstabilised DC supply should be considerably higher than the shunt stabiliser voltage.

NB Worst case conditions should be used in the above equations.

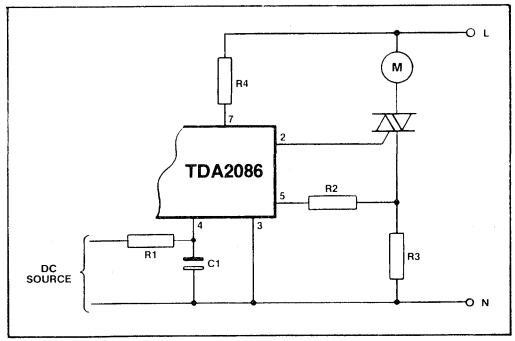


Fig.7 Operation from unstabilised DC

SYMBOLS USED IN TEXT

Symbol	Function	Units
fm	Mains Frequency	Hz
ft	Tacho Frequency	Hz
Id	Pulse Ramp Discharge Current	μA
Ir	Ramp Current	μA
Is	Supply Current	mA
Itg	Triac Drive Current	mA
K	Tacho Conversion Factor	mV/Hz
N	No. of Tacho Poles	-
Rg	Series Triac Gate Resistor	OHMS
S	Motor Speed	RPM
Vac	AC Supply Voltage (RMS)	V
Vbe	Transistor Base Emitter Voltage	V
Vcc	Negative Rail Voltage Pin 4	V
Vcr	Supply Ripple Voltage	V
Vf	Analog Feedback Voltage	V
Vp	Phase Control Voltage	V
Vr	Ramp Rate	V/s
Vreg	-5V Series Stabiliser Voltage (Pin 11)	V
Vrp	Dynamic Ramp Voltage	V
Vs	Internal Speed Reference Voltage	V
Vss	Unstabilised DC Supply Voltage	V
Vtg	Triac Gate Voltage	V
V10	Speed Program Voltage on Pin 10	V

Table 1

UNIVERSAL MOTOR APPLICATIONS

Figure 8 shows a typical universal motor closed loop speed control circuit suitable for use in domestic appliances such as food mixers or in electric drills. The circuit is basically that in the referene system diagram with the addition of component values which, with an 8 pole tacho give a speed range from zero to 15000 rev/min.

OPEN LOOP CONTROL

Where an existing tapped resistor speed control is being updated or where speed regulation is relatively unimportant, an open loop control system may be adequate and provide a lower cost solution. A basic open loop system is shown in Fig.9, but if required, the LED and current overload circuits shown in Fig.8 may be added.

OPTICAL FEEDBACK

Most applications utilise a feedback signal derived from a tacho generator but there is no reason why other systems cannot be used. Figure 10 shows how a slotted optical coupler can be interfaced with few additional components. The feedback signal is produced by interrupting the light from the LED using a perforated disc attached to the motor shaft. By connecting the LED in series with the IC, sufficient current for operation is available without increasing dissipation in the mains dropper resistor. The capacitor and resistor associated with the LED are required to provide a smooth DC supply.

CURRENT FOLDBACK

In some applications it is desirable to reduce the current overload point as the motors speed is reduced, preventing the possibility of the motor overheating due to reduced fan cooling. Figures 11 and 12 show two possible methods of achieving foldback operation, together with graphs indicating the degree of overload current reduction for various component values.

Both circuits give similar results with the exception that the version shown in Fig.12 produces a fixed current overload point at settings close to maximum phase angle. This constant overload point will extend over about 15% of the control range.

SYSTEMS INTERFACING

The 5V stabilised supply available from the TDA2086 allows standard CMOS logic elements to be powered directly thus enabling easy interface to a logic control system. Figure 13 shows a method of providing 16 speeds controlled by a 4 bit binary input from an isolated digital system. Digital information is transmitted via opto isolators to a single CMOS circuit powered from the TDA2086, any 4 bit binary counter or latch being suitable. A simple D-A converter using a CA3046 transistor array produces a 16 step analog output suitable for direct connection to the TDA2086 control input. Where only on/off control is required, this can be accomplished by connecting pin 8 to -5V by using a transistor or relay contacts as shown in Fig.14a if the current limit on pin 5 is being used or by direct connection of a CMOS gate as in Fig.14b if current limiting is not employed. This method of control discharges the ramp capacitor at switch off, allowing controlled acceleration when power is again demanded.

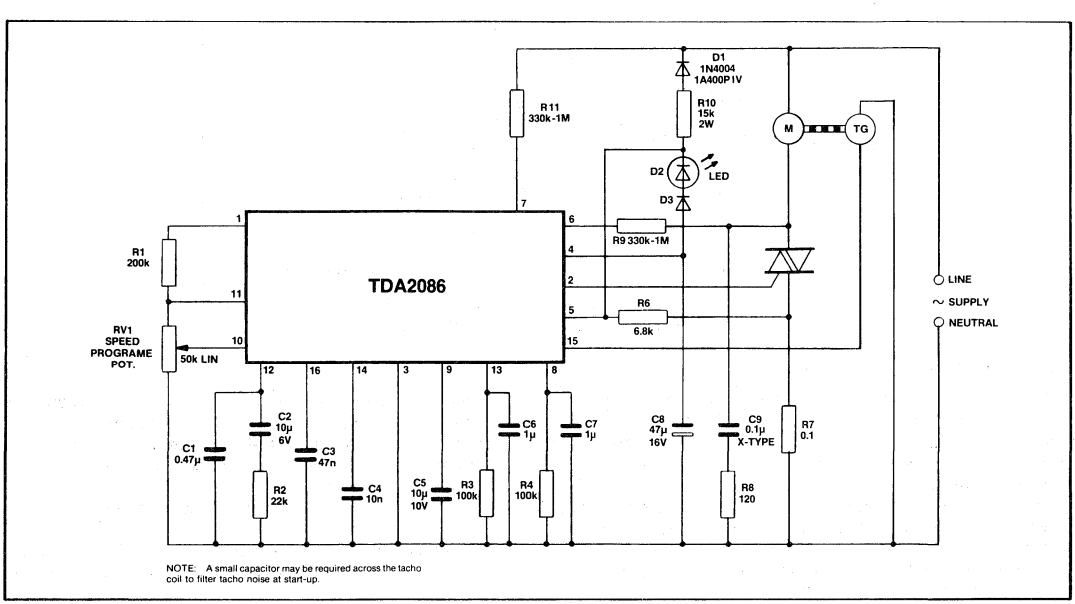


Fig.8 Universal motor application

CONTROL OF TEMPERATURE

Although the TDA2086 is primarily designed for speed control of electric motors, other types of load such as heating elements or lighting may also be controlled. Figure 15 shows a circuit for temperature control where the voltage on pin 13 set by a fixed resistor and NTC thermistor is compared with the reference voltage on pin 10. The value of Rt should be chosen to give equal voltages at pins 10 and 13 when the thermistor is at the required temperature. Care must be taken to ensure adequate RFI suppression is provided when using the TDA2086 to control resistive loads.

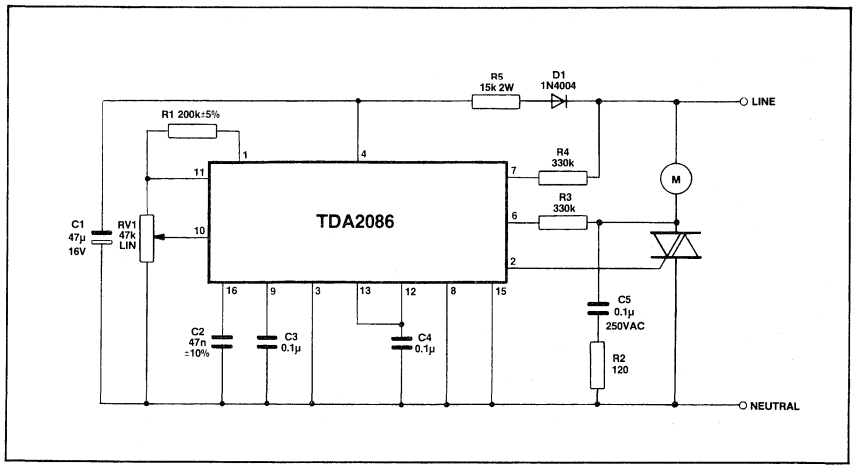


Fig.9 Open loop application, 240V

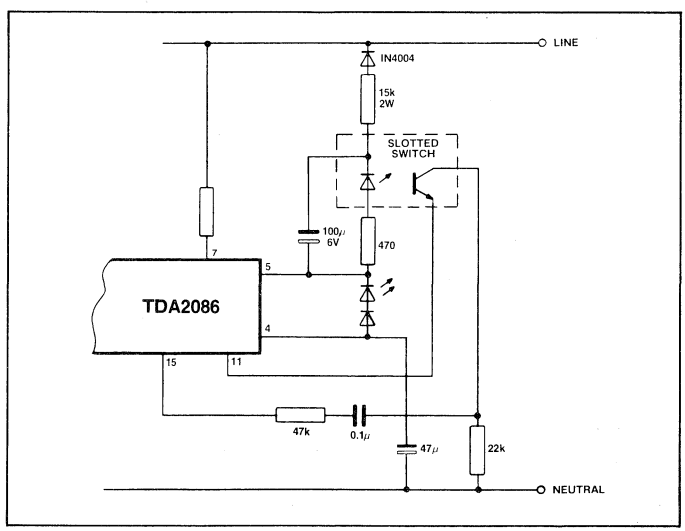


Fig.10 Optical feedback application

MOTOR REVERSING

When the TDA2086 is used in electric drills it is sometimes a requirement to reverse the direction of rotation. Unless some kind of interlock between the reversing switch and the on/off control is fitted, it is possible to damage the motor by operating the reversing switch whilst the motor is still running. To overcome this problem, it is necessary to remove power from the motor automatically when the reversing switch is operated.

It is not possible to give a precise method of achieving this as the best method depends on the design of the drill and the number of spare contacts available on the reversing switch. However in general the requirement is to rapidly discharge the soft start capacitor allowing the motor to come to rest and then to accelerate gently in the new direction.

Two methods of discharging the soft start capacitor are recommended.

1. Momentarily take pin 10 to within 50mV of the 0V rail (pin 3).
2. Momentarily take pin 8 more negative than the load current inhibit voltage with respect to pin 3. This is typically 1.5V.

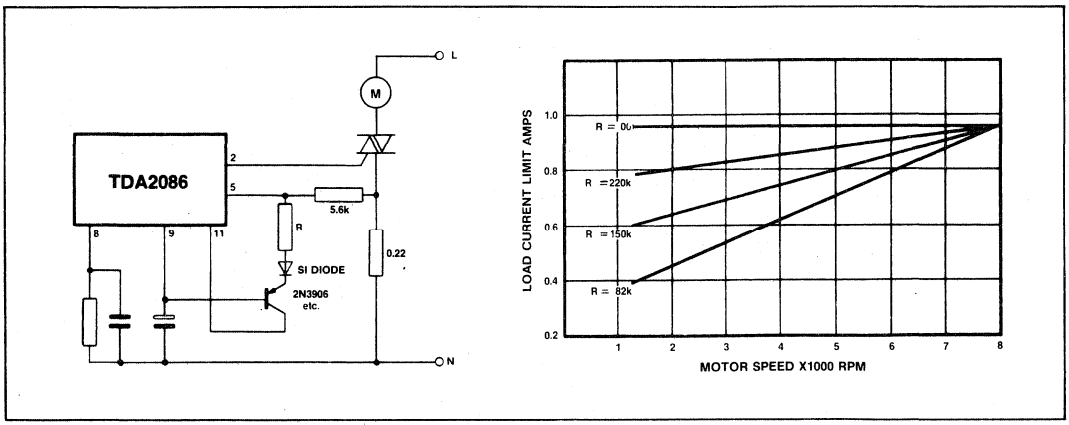


Fig.11 Current limit foldback, method 1

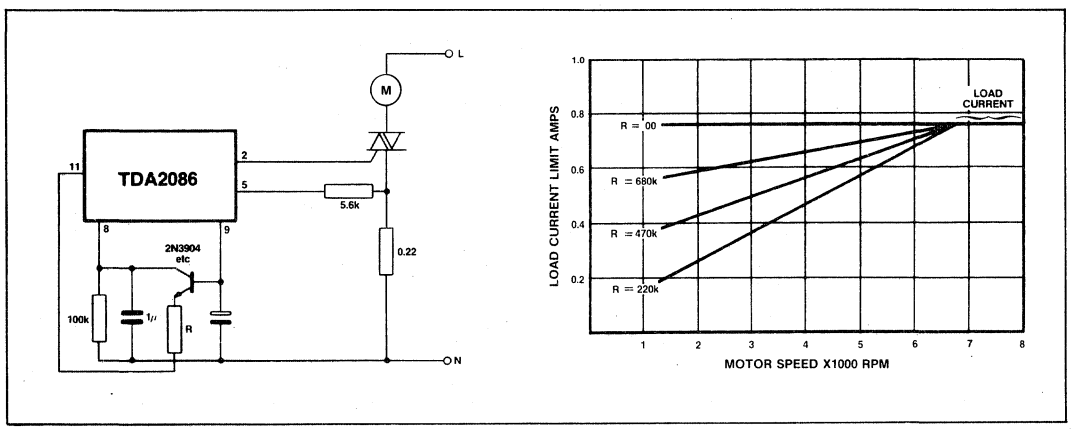


Fig.12 Current limit foldback, method 2

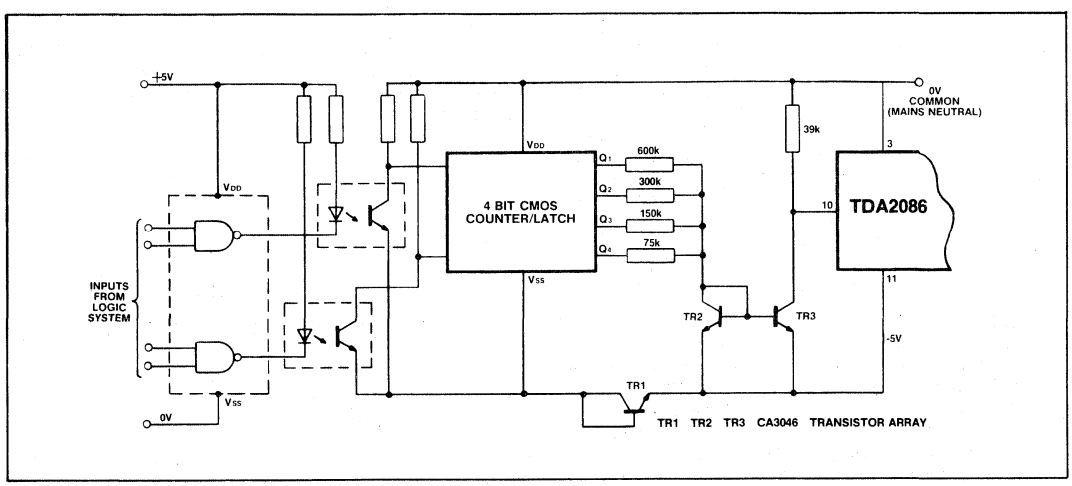


Fig.13 Interface to digital system

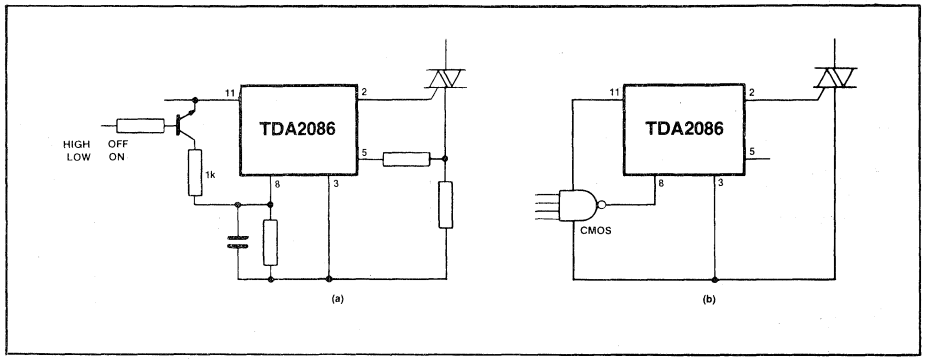


Fig.14 On/off control

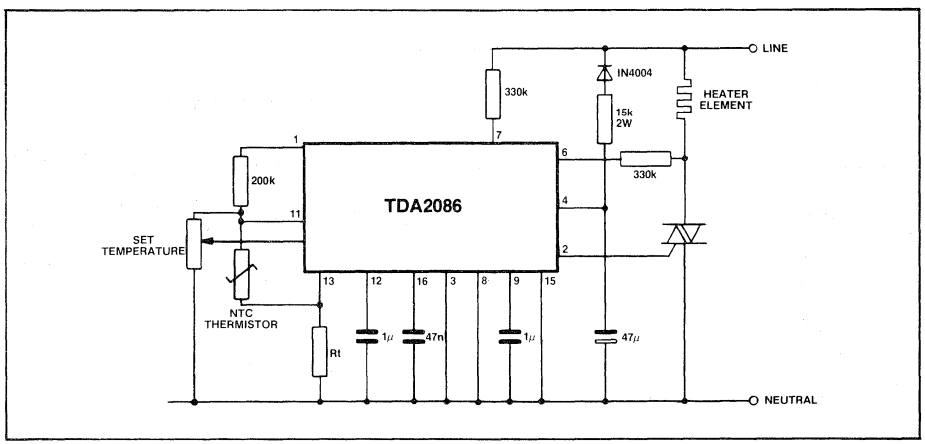


Fig.15 Temperature control application

START UP DELAY

It is sometimes possible to observe a finite time delay between the application of power to the tool and the motor starting to run. The problem is usually seen in closed loop applications and seems to affect some motors more than others.

There is no wholly satisfactory solution to this problem which is basically caused by the fact that many universal motors do not begin to turn until the applied voltage is as much as 30% of their full working voltage. At switch-on, the soft start and compensation circuit capacitors are all discharged; these capacitors must reach such a charge that the output of the error amp is about 1.5V before the motor will begin to rotate - this is the source of the time delay. Obviously, motors with large mechanical time constants (low -3dB frequency on their Bode Plot) will require heavy compensation and thus will be slow to start.

The problem can be achieved by using a different compensation circuit from the one in Fig.8. The circuit in Fig.16 applies negative feedback around the error amplifier to generate the roll-off at HF, rather than slew-limiting the output as does the circuit of Fig.8. The component values shown are typical for a large (700W) electric drill. With this circuit it was found that a satisfactory soft start was obtained without having to have a large capacitor on pin 9. The additional advantage of this technique is that no electrolytic capacitors are needed apart from the main smoothing capacitor.

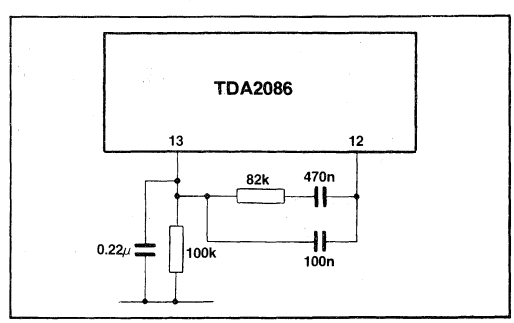


Fig.16

System Design with the TDA2088

The TDA2088 is a phase control integrated circuit optimised for current feedback control of small universal motors such as are found in small power tools and food mixers. A derivative of the TDA2086 design, it has a guaranteed minimum 100mA negative triac gate drive capability, and is thus capable of driving up to 40A triacs without pilot triacs or transistor buffers.

Figure 1 shows a typical application for variable speed control of a small universal motor.

CURRENT FEEDBACK

Figure 2 shows the feedback arrangement from Fig.1 in more detail. Component values have to be determined empirically for individual motors but the following guidelines will help.

The power dissipation in R_3 obviously has to be kept low, i.e. its value must be as low as possible, but to avoid significant speed errors from device to device the volt drop across R_3 under normal operating conditions should be >150mV so that the offset on Pin 1 (±20mV max) does not affect the feedback.

The feedback and control currents are summed at pin 6 which can draw a bias current as high as 1μA. For reasonable consistency, $V_{in}/(R_2 + Z_{out})$ should be at least 10μA at the operating speed.

Loop compensation and the integration of the feedback current pulses are effected by the capacitor C. This component should be of good quality and low leakage since it must not load the current summing node. A time constant $(R_2 + Z_{out})$ C of 0.25s is probably a good starting point for most motors. Time constants of less than 60ms should not be attempted since the ripple on the feedback component will almost certainly cause instability.

The amount of current feedback is determined by the value of R_3 and the ratio of R_4 to $(R_2 + Z_{out})$. An easy procedure to use is to determine R_3, R_2 and Z_{out} from the considerations above, choosing a large value for R_4 (very little feedback), then reduce R_4 till a satisfactory speed regulation performance is obtained.

Where variable speed operation is required it is often found that the optimum degree of feedback is different for different speeds. This problem can be reduced by using the variation in Z_{out} with control setting to alter the feedback ratio.

The circuit of Figs. 1 and 2 produces a characteristic where the feedback is at a maximum at mid-speeds and reduces at higher or lower settings. Fig.3 shows an arrangement where the amount of feedback decreases with increasing speed. Fig.4 is the converse case where feedback increases with increasing speed.

In applications where switched speeds are required (see Fig.5) then the feedback can be optimised for each speed by choosing the ratios of the resistors $R_A : R_B$, $R_C : R_D$, $R_E : R_F$, to give the desired speeds, and the values of R_A/R_B, R_C/R_D, R_E/R_F to give the desired feedback factors.

Fig.6 shows the most basic form of open-loop speed control with no current feedback.

Figs. 7 and 8 show a pcb layout and component overlay for the schematic shown in Fig.1.

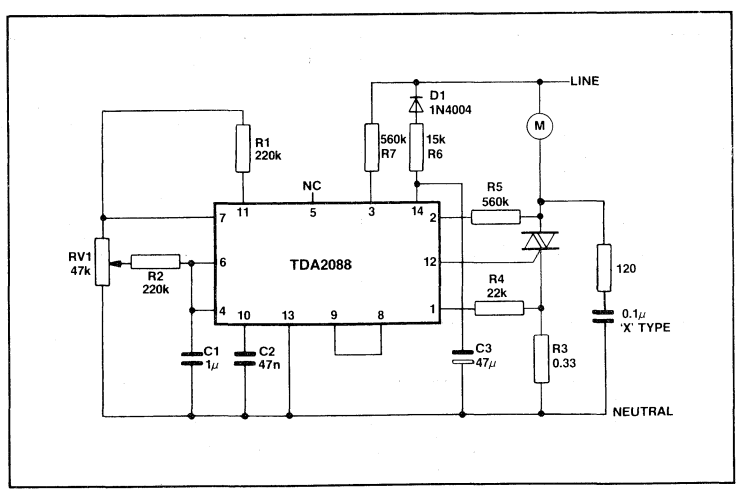


Fig.1 Universal motor speed control using current feedback

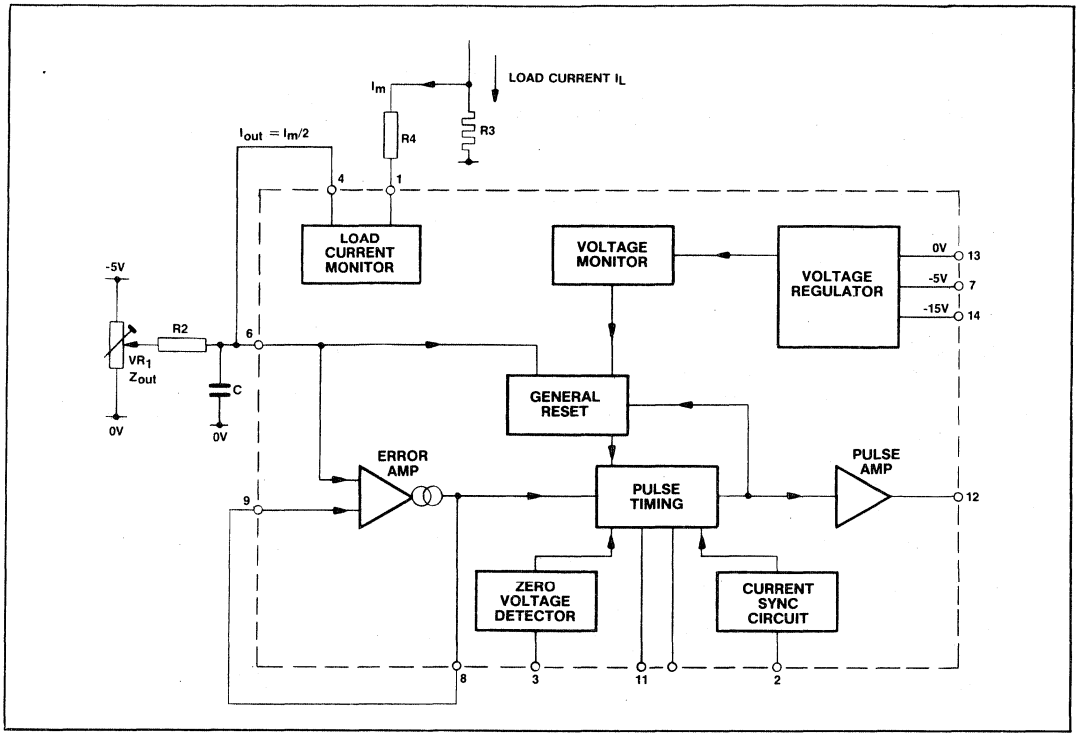


Fig.2 Feedback arrangement

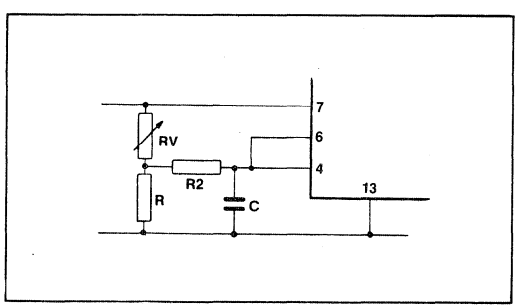


Fig.3

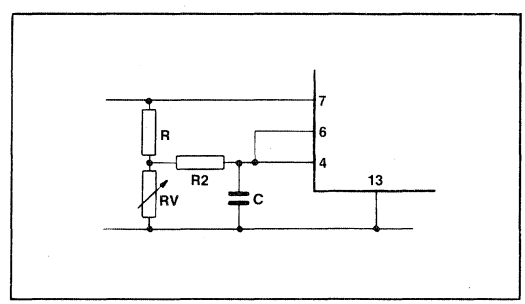


Fig.4

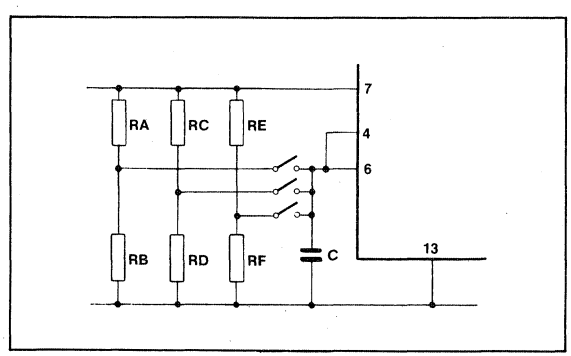


Fig.5

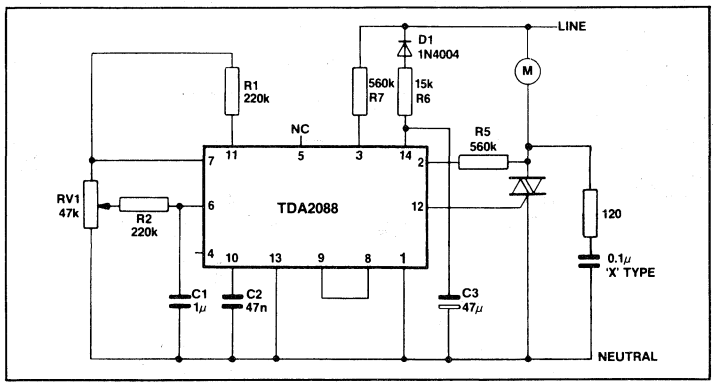


Fig.6 Open-loop speed control

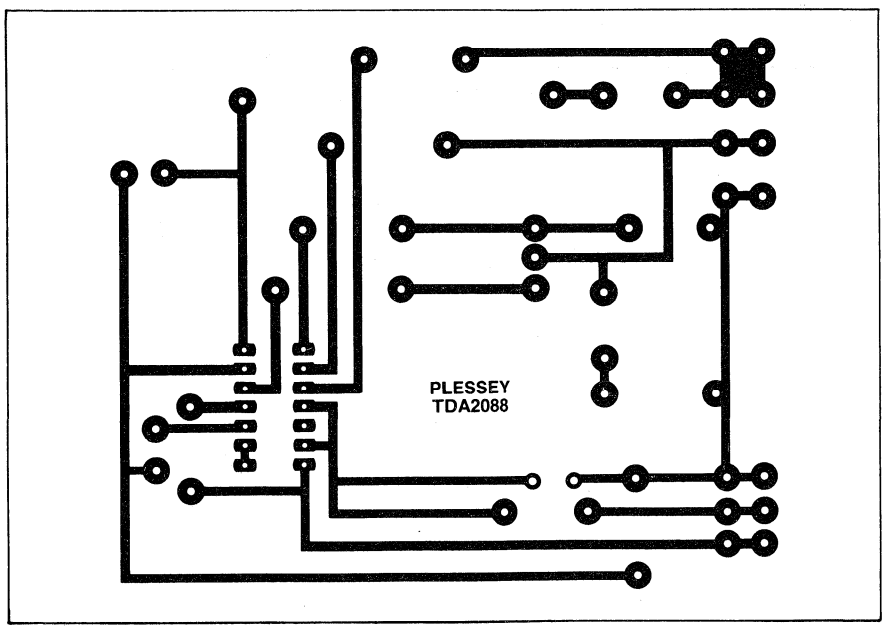


Fig.7 PCB layout for Fig.1

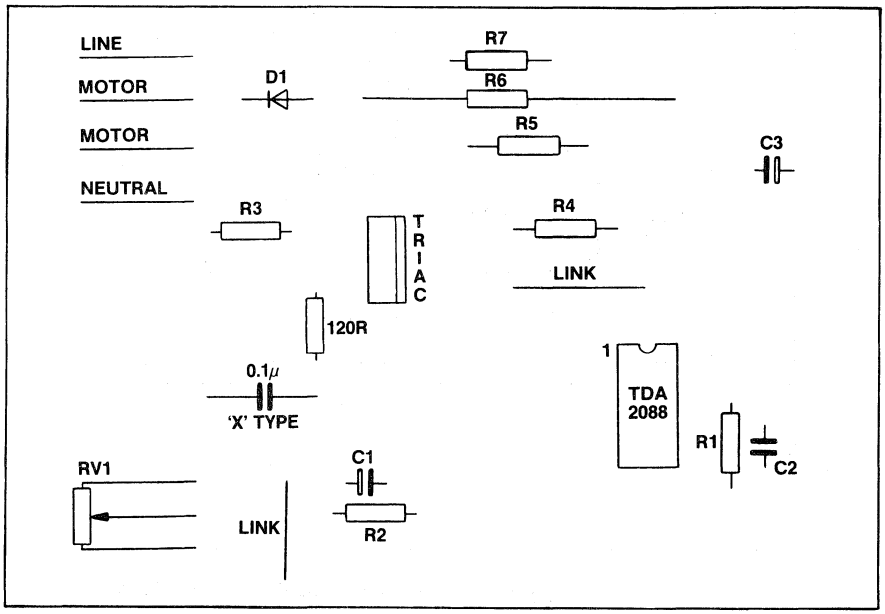


Fig.8 Component overlay for Fig.1

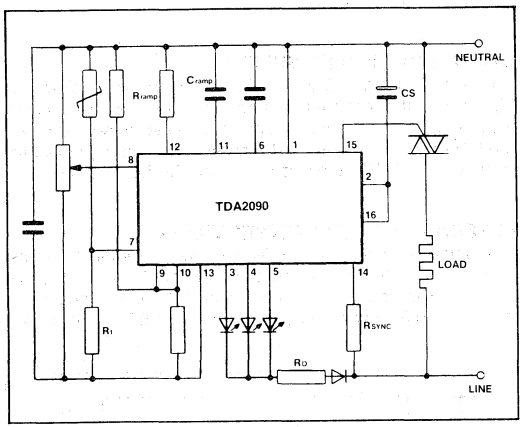


Fig.1 Basic AC mains supply application

RESISTOR R_{sync} (See Application Circuit Fig.1)

This resistor controls the width of the triac firing pulse (t_p) which is symmetrical about the mains zero crossing point as shown in Fig.2. To minimise RFI, the triac firing pulse width must be sufficient to ensure triac conduction throughout the entire mains cycle. As an example take a 1kW heating element operating from 240V AC mains using a triac with 50mA holding current (I_H).

Assuming a 5% manufacturing tolerance in the load resistance, the maximum value is given by:

$$\frac{V^2}{P} \times 1.05 = \frac{240^2}{1000} \times 1.05 = 60.48\Omega$$

The minimum mains voltage V_L required to ensure triac holding if the triac has a maximum on voltage V_t of 2V is given by:

$$V_L = I_H R_{Load} + V_t = 0.050 \times 60.48 + 2 = 5.024V$$

It is therefore necessary to ensure that the gate pulse extends beyond this point in the mains cycle in both positive and negative directions. The value of R_{sync} required to give a firing pulse of sufficient width is calculated from:

$$R_{sync} = \frac{V_L - V_{be}}{I_{sync}\ (min)} = \frac{5.024 - 0.7}{20 \times 10^{-6}} = 216.2K$$

In practice an R_{sync} value calculated for minimum triac firing pulse width in this way may sometimes produce an unacceptable high power dissipation in the sync resistor and a high peak current in the sync circuit. Since the contribution to total supply current by the triac firing pulse is small (about 0.86mA in this example) it may be advantageous to increase the value of R_{sync} somewhat to say 330K which reduces the power dissipation in R_{sync} to below 0.2W and increases the average triac firing pulse current to 1.2mA typical which is still acceptable.

AVERAGE GATE DRIVE CURRENT I_{15} (AV)

With the reservations expressed above on the value of R_{sync}, the average gate drive current should be kept to a minimum when the TDA2090 is being driven from the mains in order to reduce the power dissipated in the series dropper resistor R_D.

The maximum gate drive current is 100mA and this occurs twice each mains cycle, the average value being calculated from:

$$I_{15}(AV) = 2 \times t_p \times f \times 100mA$$

where t_p the gate pulse width is given by:

$$t_p = 2\left(\frac{V_{sync}^*}{V_m \times \sqrt{2} \times 2\pi f}\right)$$

*V_{sync} is equivalent to V_L but corrected for R_{sync} value used

Using the previous example with 330K + 10 % R_{sync} and with the maximum I_{sync} value:

$$V_{sync} = (30 \times 10^{-6} \times 363K) + 0.7V = 11.59V$$

$$t_p = 2\left(\frac{11.59}{240 \times \sqrt{2} \times 2\pi f}\right) = 217\mu s$$

$$I_{15}(AV) = 2 \times 217 \times 10^{-6} \times 50 \times 100mA = 2.17mA\ (worst\ case)$$

If necessary the triac gate drive current can be reduced by connecting a resistor in series with Pin 15.

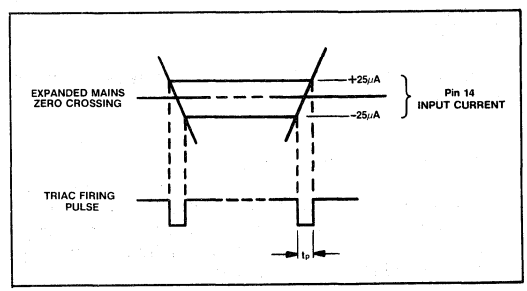


Fig.2 Firing pulse timing

MAINS DROPPING RESISTOR R_D

The value of R_D must be chosen to provide sufficient current for the IC plus the triac firing pulses and the bridge supply current on Pin 13.

Using the example above, the total DC supply current is given by:

I_{total} = 5.5 + 2.17 + 1 = 8.67mA, assuming 1mA for the bridge components.

The value of series dropper required can be calculated from:

$$R_D = \frac{Peak\ Mains\ Voltage - V_S max.}{\pi \times I_{total}}$$

where V_S max. is the zener voltage plus the voltage drop due to the LED and internal drive circuitry.

$$= \frac{240 \times 0.9 \times \sqrt{2} - 20}{\pi \times 8.67} = 10.5K\Omega$$

Specify R_D = 10K ± 5 %

The power dissipated in R_D is

$$\frac{(\sqrt{2}\,V_{ac} - V_{cc})^2}{4R_D\ min.}\ Watts$$

$$Maximum\ Power\ in\ R_D = \frac{(\sqrt{2} \times 240 \times 1.1 - 14)^2}{4 \times 0.95 \times 10000} = 3.4W$$

MAINS SMOOTHING CAPACITOR C_s

The smoothing capacitor C_s should be chosen to give a supply ripple of less than 2V pk using the formula:

$$C_s = \frac{I_{total}}{V_{ripple} \times f_m} \times 10^3 = \frac{8.67}{2 \times 50} \times 10^3 = 86.7\mu F$$

Specify 100μF - 20 % + 100 %.

RAMP GENERATOR COMPONENTS C_{ramp} and R_{ramp}

These components determine the switching rate of the power applied to the load in the proportional control band. The rate of switching should be chosen to comply with EN50.006 and BS5406, 1976.

The capacitor value is given by:

$$\frac{It}{10} \times 10^6 \mu F$$

where t is the switching time in seconds and I is the capacitor charge current given by

$$I = \frac{V_{reg} - 0.7}{R_{ramp}}$$

The ramp current should be limited to between 5 and 50 micro-amps.

THERMISTOR BRIDGE CIRCUIT

The simple bridge circuit shown in Fig.1 uses a minimum number of components but has the disadvantage that the control range is effectively infinite. To limit the control range to that required it is usually necessary to introduce end-stop resistors R_a and R_b as shown in Fig.3.

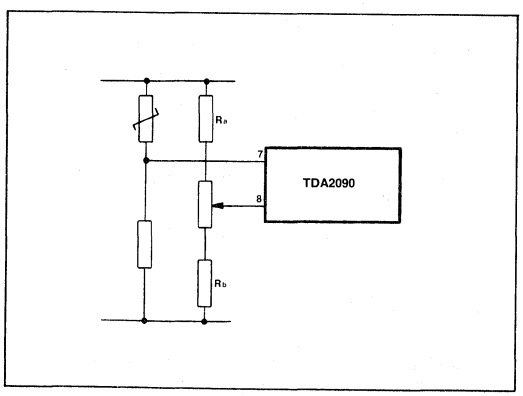


Fig.3

The resistor R_t in the thermistor arm is usually chosen for best linearity of the control potentiometer over the required temperature range.

When choosing thermistor bridge components, care must be taken to keep the bridge supply current to a reasonable level particularly at high temperatures when the thermistor resistance is low. If unsuitable thermistor and R_t values are selected, the voltage at pin 7 may fall below the open circuit sensor trip level at low temperatures preventing any power from reaching the load.

OPERATION FROM DC SUPPLY

Operation from DC is possible provided the voltage is higher than the maximum voltage monitor enable level and lower than the circuit maximum rating. Due to the design of the LED drive circuit, the LEDs must be driven in parallel as shown in Fig.5. R_L being used to limit the LED current.

ALTERNATIVE LED CONNECTIONS

In some applications 3 LEDs may not be required. In this case it is possible to combine several outputs onto one LED or to connect one or more outputs so that no LED indication is given. Fig.6 shows various methods of LED connection.

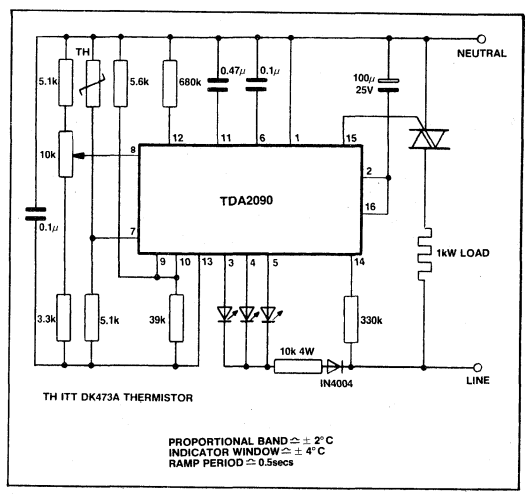


Fig.4 Application for 50-100°C temperature control

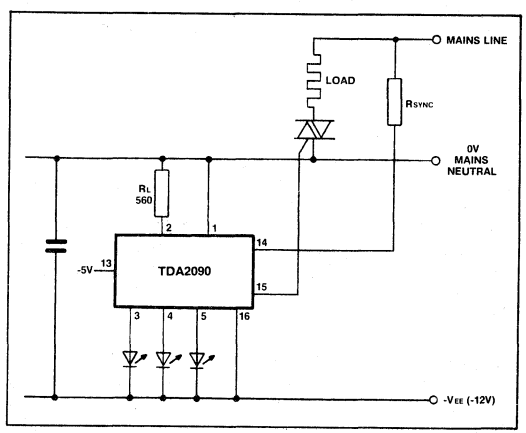


Fig.5 DC supply application

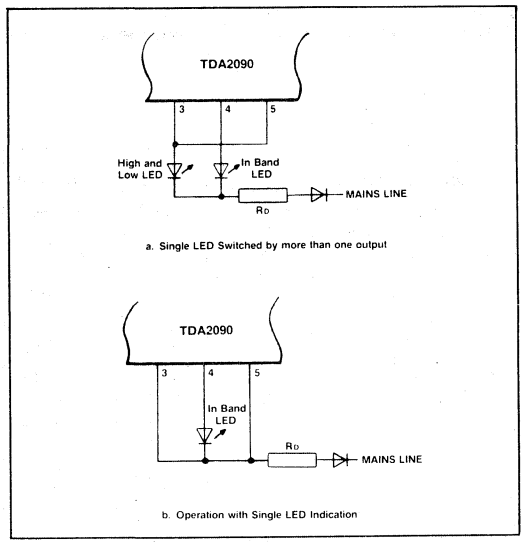


Fig.6 Alternative LED connections

OPERATION WITHOUT PROPORTIONAL BAND

When only on/off control is required, a saving in external components may be made, as the ramp generator timing components are not necessary. In this case, Pin 9 is connected to common and Pins 11 and 12 connected to -5V.

System Design using the ZN409

OPERATING AND DESIGN NOTES

1. SERVO APPLICATION

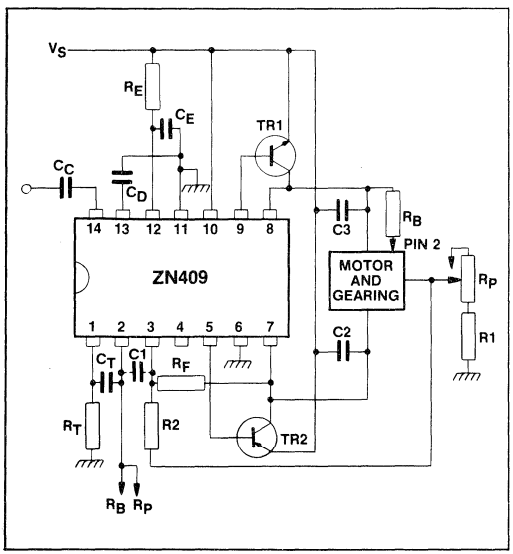


Fig.1 Servo system reference diagram

Component function	Circuit reference	Value	Comments
Monostable timing components	R_T C_T	100kΩ 0.1μF	Note 1(e)
Potentiometer and timing reference components	R_P R_1	1.5kΩ 5kΩ 4.7kΩ	Note 1(e) Note 1(g) Note 1(e)
Pulse expansion	C_E R_E	0.47μF 180kΩ 150kΩ	Note 1(d) 11Ω motor 8Ω motor
Deadband (Note 1(c))	C_D	1000pF 1500pF	11Ω Motor 8Ω motor
Dynamic feedback	R_F R_B R_2	330kΩ 330kΩ 1.2kΩ	 Note 1(f)
Input coupling	C_C	2.2μF	Note 1(b)
Motor decoupling	C_2 C_3	0.01μF 0.01μF	
RF decoupling	C_1	0.1μF	Note 1(h)
Drive transistors	TR_1, TR_2		Note 1(i)

Table 1 Components for Fig.1

(a) Introduction

In the standard servo application the displacement of a control stick varies the pulse width of a timing circuit and many such pulses are time division multiplexed and typically modulate a 27MHz transmitter. A receiver then decodes the transmitted signal and reconstitutes an independent train of pulses for each servo channel. The servo shown in Fig.4 consists of the ZN409 integrated circuit several external components, a power amplifier consisting of two external PNP transistors and two on-chip NPN transistors which form a bridge circuit to drive the DC motor. The motor drives a reduction gearbox which has a potentiometer attached to the output shaft. This potentiometer in association with R_1 and the timing components C_T and R_T controls the pulse width of the timing monostable. The input pulse is compared with the monostable pulse in a comparison circuit and one output is used to enable the correct phase of an on-chip power amplifier. The other output from the pulse comparison circuit drives the pulse expansion circuit (C_E, R_E) via the deadband circuit (C_D). Thus any difference between the input and monostable pulses is expanded and used to drive the motor in such a direction as to reduce this difference so that the servo takes up a position which corresponds to the position of the control stick.

(b) Input Circuit

The ZN409 operates with positive going input pulses which can be coupled either directly or via a capacitor to pin 14. The advantage of AC coupling is that should a fault occur in the multiplex decoder which causes the input signal to become a continuous positive level, the servo will remain in its last quiescent position, whereas with direct coupling the servo output arm will rotate continuously. A nominal 27kΩ resistor is shunted across the input on chip to provide DC restoration of the input signal when AC coupling is used. The active input circuit is a Schmitt trigger which allows the servo to operate consistently with slow input edges and supplies the fast edge required by the trigger monostable independent of input edge speed.

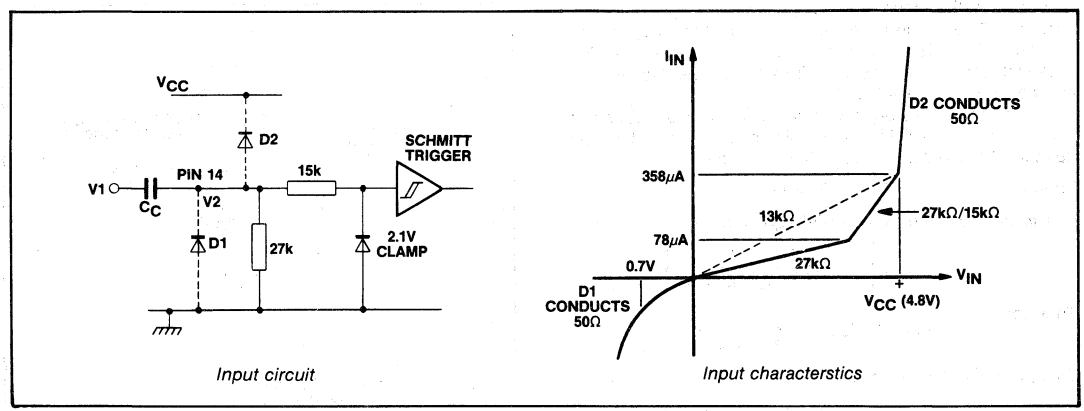


Fig.2

The input circuit and its V/I characteristic are shown in Fig.2. D_1 and D_2 are the parasitic substrate and isolation diodes associated with the input resistors. It is advisable that the pulse input amplitude should not fall below 0V nor exceed the supply voltage V_{CC} in order to prevent these diodes from conducting, although a small amount of conduction will not cause the circuit to malfunction. When AC coupling is used the value of C_C should be chosen to give a pulse droop not exceeding 0.3V.

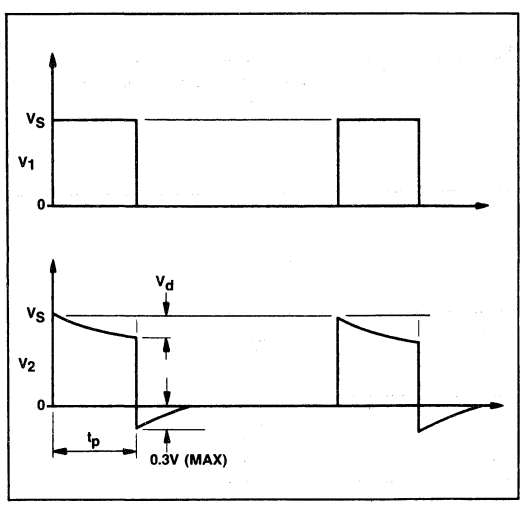


Fig.3 Input waveforms

Assuming that the input signal swings between 0V and V_S and taking the input chord resistance R_{IN} of 13kΩ, the droop for a pulse of duration t_p ms will be:

$$V_d = \frac{V_S\, t_p}{C_C \times R_{IN}} \text{ volts}$$

where t_p is in ms, C_C in μF and R_{IN} in kΩ.

For a nominal pulse width of 1.5ms and V_d equal to 0.3V the required minimum value of C_C can be found as follows:

$$C_C = \frac{4.8 \times 1.5}{0.3 \times 13} = 1.85\mu F$$

A nominal value of 2.2μF is chosen (nearest preferred value).

If it is required to operate the servo with reduced input pulse amplitude the input pulse should exceed the upper Schmitt threshold voltage of 1.5V by a reasonable margin and a minimum input pulse amplitude of 2.4V is recommended.

(c) Deadband Circuit

The function of the deadband circuit is to provide a small range of output shaft position about the quiescent position where the difference pulse does not drive the motor. This is necessary to eliminate hunting around the quiescent position caused by servo inertia and overshoot. The minimum deadband required is also a function of the pulse expansion characteristics and dynamic feedback component values.

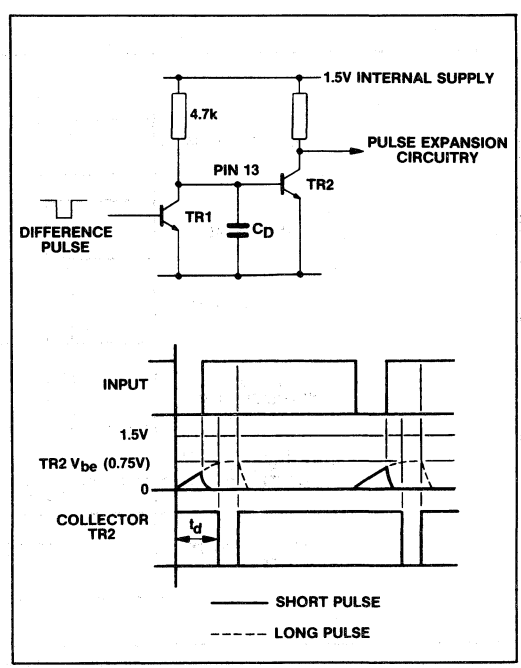


Fig.4 Deadband circuit and waveforms

When the difference pulse is applied TR_1 turns off and the base of TR_2 rises on an exponential waveform with a time constant of 4.7kΩ x C_D. If the difference pulse is small the potential reached on the base of TR_2 is insufficient to turn TR_2 on and no output results.

The pulse expansion circuit has a built in deadband of 1.5μs with C_E = 0.47μF and this must be added to the deadband caused by C_D to obtain the total T_d.

Therefore $T_d = 1.5 + t_d \mu s$

t_d is found from the exponential equation.

$$V_{be} = V_1 \left[1 - \exp\left(\frac{-t_d}{C_D \times 4.7k\Omega}\right)\right]$$

Therefore

$$t_d = C_D \times 4.7 \log_e \left(\frac{V_1}{V_1 - V_{be}}\right)$$

Therefore $= 3.3\ C_D \mu s$ (C_D in nF)

(Taking V_1 = 1.5V and V_{be} = 0.75V)

Thus with C_D equal to 1000pF (1nF) t_d = 3.3μs and T_d = 4.8μs.

The mechanical deadband Φd depends on the chosen sensitivity S_1 of the servo and in the usual radio control application a ±500μs input pulse variation ±50° rotation, i.e. S_1 = 10μs per degree.

Thus $\Phi d = \frac{2 \times 5_d}{S_1}$ degrees (T_d in μs. S_1 in μs per degree).

Thus a value for T_d of 5μs provides a mechanical deadband Φd of 1°.

And generally:

$$\Phi d = \frac{2 \times (1.5 + t_d)}{S_1}$$

$$\Phi d = \frac{3 + 6.6\ C_D}{S_1} \text{ degrees } \begin{cases} C_D \text{ in nF.} \\ S_1 \text{ in } \mu s \text{ per degree.} \end{cases}$$

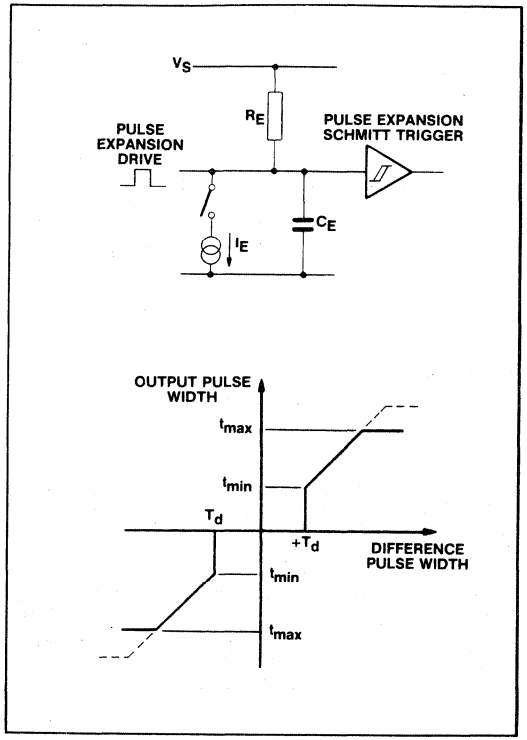


Fig.5 Pulse expansion circuit and characteristic

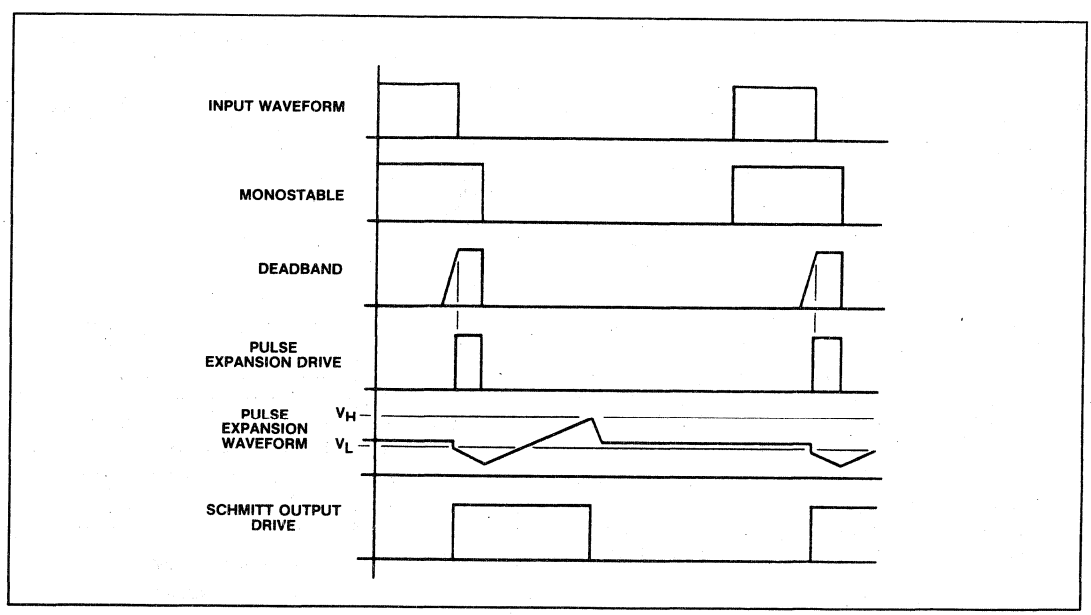


Fig.6 Pulse expansion timing diagram

(d) Pulse Expansion

A schematic of the pulse expansion circuit is shown in Fig.5. In the quiescent state ith no drive the Schmitt trigger input is biased via R_E and takes up a level just above the lower threshold V_L.

A drive pulse causes a current I_E to be switched on for the duration of the pulse and this discharges C_E linearly with time. Thus, at the end of the pulse the voltage on C_E depends on the duration of the pulse. If the pulse is narrow and just causes the potential on C_E to fall to V_L the Schmitt trigger will switch to the upper threshold V_H and at of the drive pulse C_E will start to charge to V_H with a time constant $C_E R_E$. When the potential on C_E reaches V_H the Schmitt will switch to V_L and C_E will discharge to the quiescent level. The output drive is taken from the Schmitt output.

DC motors need a certain amount of drive to overcome static friction and the minimum output pulse obtained from this form of pulse expansion characteristic is chosen to ensure that the motor will rotate when driven. A linear initial pulse expansion characteristic would result in the motor remaining stationary and drawing full stall current for small drive periods. If the motor needs 2ms of drive at a repetition rate of 20ms to cause rotation, this is equivalent to an average drain of 50mA for a 0.5A stall current. This is many times more than the quiescent current of the ZN409 (7mA) and could considerably reduce flying time for the standard battery operated airborne multichannel radio control system. This effect also causes an annoying buzz from the motor and gearbox. The use of the Schmitt trigger removes these two deficiencies.

The value of t_{min} is determined by the Schmitt trigger hysteresis and the exponential waveform on C_E in the following equation.

$$V_H = (V_{CC} - V_L)\left[1 - \exp\left(\frac{-t_{min}}{C_E R_E}\right)\right]$$

because V_H is small the following linear relationship is sufficiently accurate.

$$V_H = \frac{(V_{CC} - V_L)}{C_E R_E} \times t_{min}$$

Therefore

$$t_{min} = \frac{V_H}{(V_{CC} - V_L)} \times C_E R_E \text{ ms}$$

For nominal operation $V_{CC} = 4.8V$; $V_L = 1.5V$; $V_H = 0.12V$ and:

$$t_{min} \simeq \frac{C_E R_E}{30} \text{ ms}$$

where C_E is in μF and R_E is in $k\Omega$; for $C_E = 0.47\mu F$ and $R_E = 180k\Omega$, $t_{min} = 3.5ms$.

It can be seen from the simple equation that t_{min} is dependent on V_{CC}, and t_{min} will increase with reducing V_{CC}. This variation is put to good use to maintain the initial motor drive, $V_{CC} \times t_{min}$ reasonably constant over the operating voltage range of 3.5 to 6.5V.

When the pulse expansion drive is increased above the minimum value the output pulse increases from t_{min} almost linearly until full pulse expansion is reached, i.e. when the output pulse width equals the input pulse repetition rate. The pulse expansion will be almost linear provided that the current source I_E does not saturate, i.e. provided that C_E is not discharged to almost zero volts. Ideally the current source should saturate when full motor drive is obtained but due to component tolerances it is usual to allow some margin to ensure that full motor drive can be obtained. If a margin is allowed, an extended pulse expansion characteristic results (shown dotted in Fig.5) and if this is excessive it can lead to the servo exhibiting an underdamped characteristic causing jittering or hunting. Thus for full pulse expansion the voltage on C_E should discharge from its quiescent value of 1.5V to 0.75V. Thus with $I_E = 3mA$ for the current source:

$$\frac{1.5 - 0.75}{t_e} = \frac{I_E}{C_E}$$

Therefore $C_E = 4t_e \mu F$ (t_e in ms)

For $t_e = 0.1ms$, a value of $0.47\mu F$ was chosen for C_E.

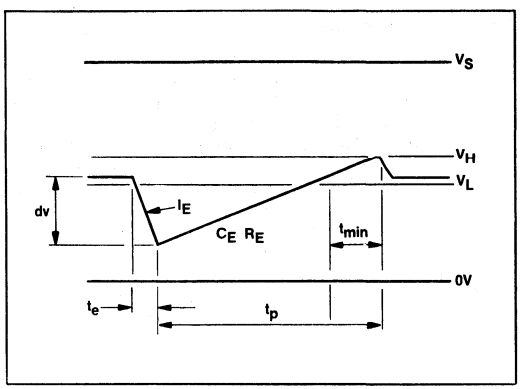


Fig.7 Pulse expansion waveform

If t_p is the maximum motor drive pulse length required, i.e. equal to the input pulse repetition period for full pulse expansion, and the mean value of the potential on C_E is taken as 1.2V, then:

$$dv = \frac{(t_p - t_{min})}{C_E R_E} \times (V_{CC} - 1.2)$$

And for the discharge period t_e:

$$dv = \frac{I_E \times t_e}{C_E}$$

Therefore

$$R_E = \frac{(t_p - t_{min})}{I_E t_e} \times (V_{CC} - 1.2)$$

For nominal values of $V_{CC} = 4.8V$ and $I_E = 3mA$

$$R_E = 1.2 \frac{(t_p - t_{min})}{t_e} \text{ k}\Omega$$

and for $t_p = 20ms$, $t_{min} = 3.5ms$, $t_e = 0.1ms$, $R_E = 180k\Omega$ (nearest preferred value).

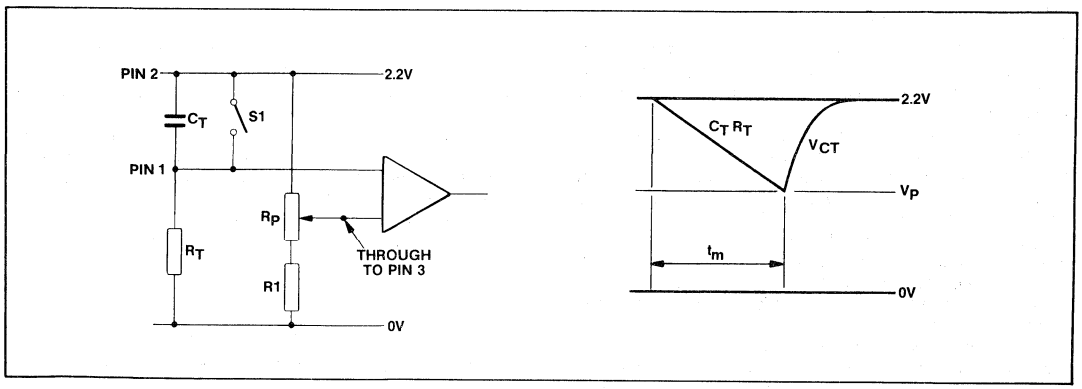


Fig.8 Monostable timing circuit and waveform

(e) Monostable Timing

The leading edge of the input waveform triggers the timing monostable by opening switch S_1. C_T then charges until the differential amplifier detects that the timing waveform potential has fallen to V_P, the potential on the potentiometer wiper and switch S_1 is closed to terminate the timing pulse. Thus the monostable period is determined by setting of the potentiometer wiper. In the standard application the servo centre position pulse width is 1.5ms with a range of $\pm 50°$ rotation at $10\mu s$ per degree. Thus the 2.0ms maximum monostable period $t_{mono(max)}$ corresponds to a potentiometer setting of 200° (for a linear relationship) and since the potentiometer has a total rotation of approximately 270° and the maximum allowable swing on pin 3 is specified as 0.5V the value of $C_T R_T$ can be calculated as follows:

$$\frac{0.5}{t_{mono(max)}} \simeq \frac{2}{C_T R_T}$$

Therefore $C_T R_T = 4\ t_{mono(max)}$

Thus if $t_{mono(max)} = 2ms$, $C_T R_T = 8ms$.

The optimum value of R_T is 100kΩ due to the design of the on-chip monostable circuit, giving $C_T = 0.1\mu F$ (nearest preferred value).

$$R_T = 100k\Omega \qquad C_T = 0.1\mu F$$

The value of R_1 can now be calculated from the actual voltage swing with a potentiometer setting of $\Phi p = 200°$ and $\Phi max = 270°$.

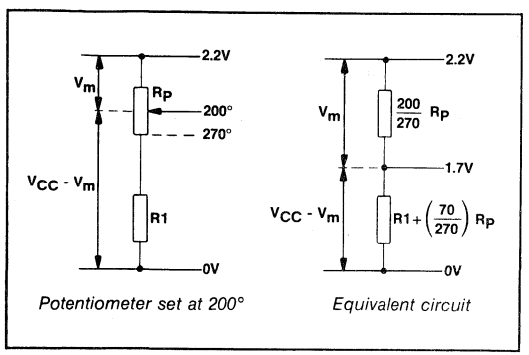


Fig.9

Thus from the equivalent circuit,

$$\frac{V_m}{\frac{200}{270} \times R_P} = \frac{(V_{CC} - V_m)}{R_1 + \frac{70}{270} R_P}$$

where V_m is calculated from the actual values of C_T and R_T chosen using the relationship

$$V_m = \frac{2.0 \times t_{mono(max)}}{C_T R_T}$$

since $C_T = 0.1\mu F$ (nearest preferred value) was chosen with $R_T = 100k\Omega$, $V_m = 0.4V$ and hence

$$R_1 = 3.1\ R_P$$

If $R_P = 1.5k\Omega$ then $R_1 = 4.7k\Omega$.

(f) Dynamic Feedback

Without dynamic feedback in the standard application the inertia of the motor and gearbox causes the servo output shaft to overshoot the set position which results in the servo 'hunting'. If the deadband was widened to stop this effect an unacceptably large deadband would result and the servo would still be underdamped. The dynamic feedback circuit utilises the motor back emf (which is proportional to motor speed) and feeds back a proportion of this signal to the wiper of the potentiometer. The phase of the feedback signal is chosen to modify the potential on the wiper so that the monostable period is dynamically varied to reduce the motor drive as the servo output shaft approaches the set position and the values of the feedback resistors are chosen to achieve optimum settling characteristics.

The value for R_F and R_B of 330kΩ will suite the normal type of servo mechanism, however if the servo is fairly fast this can be decreased to 300kΩ to minimise any tendency to overshoot. Where the servo is slow R_F and RB can be increased to 360kΩ or 390kΩ.

(g) Alternative Value of R_P

Although a 1.5kΩ feedback potentiometer is the most common value of R_P, 5kΩ potentiometers are used in some servo mechanisms. In order to use this value with the ZN409 a 2.2kΩ resistor is usually connected across the potentiometer to maintain the values of R_F and R_B at 330kΩ and R_1 at 4.7kΩ. R_2 is omitted, i.e. the wiper of the potentiometer is connected directly to pin 3 of the ZN409.

(h) RF Decoupling

C_1 (typical value 0.1μF) is only necessary where strong RF fields may affect the operation of the circuit.

(i) Transistors TR_1 and TR_2

The external PNP transistors are usually selected for a low $V_{CE(sat)}$ to obtain a maximum output drive and the recommended types are the ZTX550 or ZTX750.

2. MOTOR SPEED CONTROL

In the motor speed control application the ZN409 is used as a linear pulse width amplifier. The DC motor is driven via a power amplifier with a train of pulses whose mark/space ratio can vary between zero and unity to control the motor speed from zero to maximum. The ZN409 operates with fixed timing components and a fixed resistor replaces the position feedback potentiometer. The nominal monostable period represents zero motor speed and input pulses less than or greater than nominal drive the motor in the forward and reverse direction respectively. The motor direction is usually controlled by a relay operated from pin 4, the direction output. Pulse expansion components C_E and R_E are chosen to obtain the required relation between control stick deplacement and motor speed and it is usual to operate with a much larger deadband than that used in the servo application.

Because high current motors are used to drive the wheels of model cars or propellers of model boats a separate supply of 6 to 12V is used, and to provide reasonable running time between recharging the battery, a capacity of 1.2AH is usual.

One twelfth scale cars with reasonable performance can be powered by a 5A stall current motor such as the 'Marx Monoperm' (6-12V) driven from a single 2N3055 power transistor. However, if very high performance is required then five or six 2N3055 power transistors are used in parallel as shown in Fig.10 to drive a 25A stall current motor. The 'Mabuchi RS54' operates from 6 to 8V and will provide a top speed of about 25 mph in a one eighth scale car. Acceleration is superb and the car wheels can be spun easily even on the best surfaces although the 1.2AH battery will need a full recharge after some ten minutes of racing. The motor and 2N3055 transistors dissipate a great deal of power especially at low speed and almost full stall current drive so the power transistors need to be mounted on a good heat sink such as the aluminium chassis of the care and a motor with crimped commutator connections rather than soldered connections is necessary since soldered connections have been seen to melt under stall conditions.

The outputs from pins 9 and 5 of the ZN409 integrated circuit are combined using two ZTX502 PNP transistors to provide a pulsed output whose mark/space ratio varies from zero to unity depending on the deflection of the control stick. This signal is then used to drive the motor via the power amplifier.

The ZN409 has additional circuitry which performs the motor reversing function by taking the output from the direction bistable and provides either zero current or approximately 3mA sink current at pin 4, depending on the state of the direction bistable. This current is amplified and used to drive the relay coil (100mA) via the ZTX450 transistor thus controlling the motor direction via the relay changeover contacts.

It is usual to have a relatively wide deadband and C_D = 0.022μF provides a deadband of about 14% (±7 degrees).

The pulse expanision components C_E and R_E are chosen to give full motor drive at about 90% full stick displacement and using the formulae derived earlier yields values of C_E = 1μF, R_E = 82kΩ. The monostable timing component values remain unchanged at C_T = 0.1μF, R_T = 100kΩ. A 1kΩ potentiometer (R_P) can be used to set up the zero output condition with the control stick in its central position.

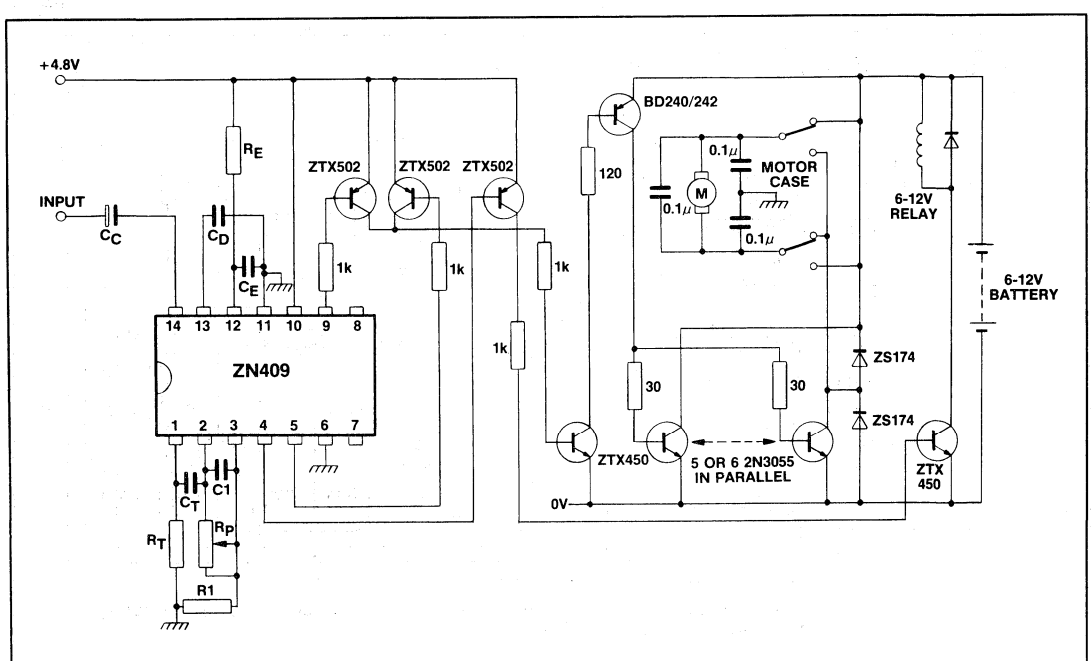


Fig.10

Component function	Circuit reference	Value
Monostable timing components	R_T	100kΩ
	C_T	0.1μF
Potentiometer and timing reference components	R_P	1kΩ
	R_1	4.7kΩ
Pulse expansion	R_E	82kΩ
	C_E	1μF
Deadband	C_D	0.022μF
Input coupling	C_C	2.2μF
Motor decoupling. See Note 1(h)	C_1	0.01μF

Table 2 Components for Fig.10

3. SERVO SYSTEM FOR MEDIUM POWER SERVO MOTORS

The ZN409 is a precision monolithic integrated circuit designed particularly for pulse width modulated position servo mechanisms used in all types of control applications. The basic circuit for a servo system (shown in Fig.1) is suitable for small servo motors up to a rating of 6V, 0.5A, as are found in the normal model control servos in popular use. This section describes a circuit suitable for driving more powerful servo motors for industrial and professional control applications. The circuit was designed for a 24V, 2A motor, but it can easily be modified for motors of different power ratings.

The circuit diagram of the system is shown in Fig.11 and a PCB layout is shown in Fig.12. The output drive is taken from the PNP Base Drive outputs of the ZN409 and applied to transistors TR_1 and TR_2. These transistors drive the inputs of a bridge power amplifier comprising TR_3, TR_5 TR_8 on one side and TR_4, TR_6 and TR_7 on the other. The amplifier operates in the fully saturated mode so the power to the motor, connected across the bridge output, is determined by the pulse width of the ZN409 output. Under quiescent conditions the ZN409 output pins 5 and 9 are switched off, keeping transistors TR_1 and TR_2 turned off. With no base drive TR_3 and TR_4 are also turned off, as are all four output transistors TR_5 to TR_8. When there is sufficient difference between the input and internal monostable pulse widths either pin 5 or pin 9 will go low for a period as determined by the pulse expansion characteristic. Assume that the input pulse width is less than the internal mono pulse width, in which case pin 5 will go low. This will turn on TR_2 which in turn will switch on TR_4. Transistor TR_4 will supply base current drive to TR_6 and TR_7 driving them both into saturation. Hence current will flow from the positive rail via TR_7, through the motor, and then TR_6 down to the 0V rail. Hence the motor will drive the servo pot, in a direction which should reduce the internal mono pulse width until this is equal to the input pulse width ± the deadband value. Conversely, if the input pulse width is greater than the internal mono pulse width then output transistor TR_5 and TR_8 will be turned on and the motor will rotate in the opposite direction.

The part of the circuit comprising D_1, D_2, TR_9, R_8, R_9, R_5 and RV_5 enables a minimum output pulse width of less than 1ms to be obtained instead of the 3.5ms minimum pulse from the standard circuit. This operates by switching TR_9 on for several milliseconds at the start of each output pulse. This switches $R_5 + RV_5$ to +5V thereby modifying the CR time constant of the pulse expansion circuit. RV_5 provides adjustment of the minimum pulse width. This was found to

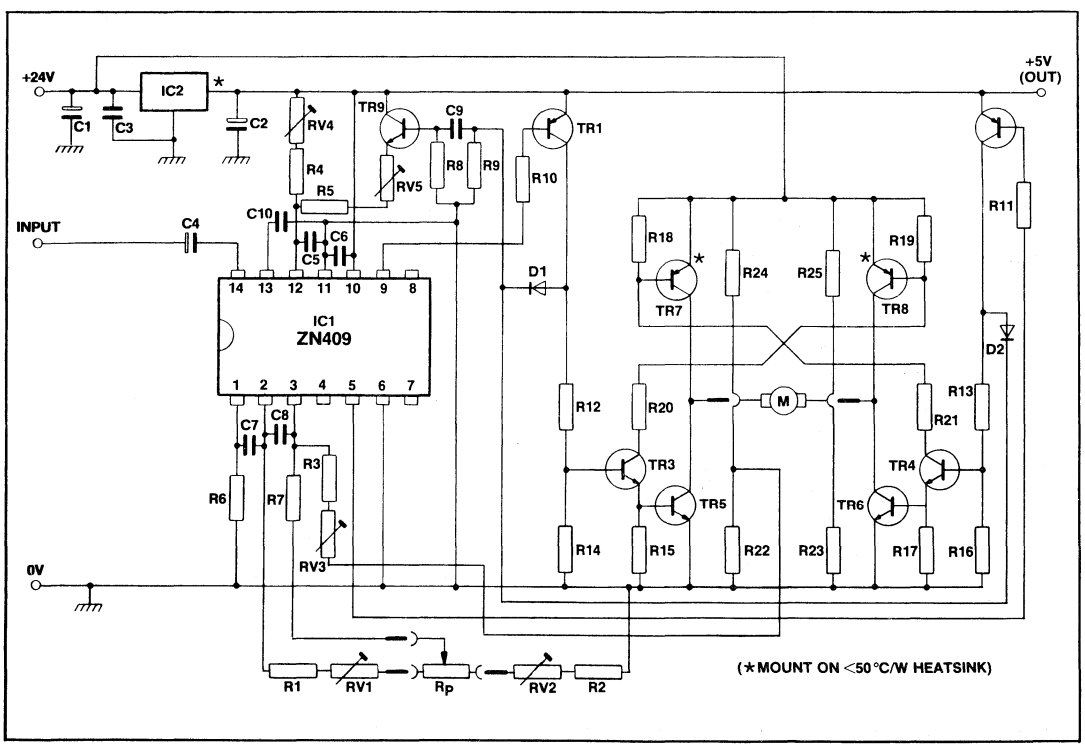


Fig.11

be necessary on precision servos with low inertia rotors requiring low starting torque. Too wide a pulse drive causes coarse jerky output and can produce instability problems.

Potentiometer RV_4 was added to provide some gain adjustment. C_5, the pulse expansion capacitor, was doubled from its standard value to ensure a linear expansion characteristic with lower values of RV_4.

The value of the velocity feedback resistor $R_3 + RV_3$ has been increased commensurate with the increased supply voltage to the motor. RV_3 provides adjustment of the servo response, too high a resistor value results in overshoot and instability, too low a value produces sluggish response and 'creep'.

Incorporation of the 5V regulator IC_2, allows operation from a single supply rail. This can be omitted if dual supplies are available.

The control range of the servo is determined by the resistance of the servo position potentiometer in conjunction with the end resistors $R_1 + RV_1$ and $R_2 + RV_2$. For example assume the full angular range of a 2kΩ servo pot. is required with the standard RC pulse width of 1.5ms ± 0.5ms. The range of change of voltage across the timing capacitor C_T can be approximated to:

$$\frac{dV_C}{dT_{mono}} = \frac{V_S}{C_T \times R_T}$$

where V_S = Pin 2 supply voltage = 2.2V
C_T = Timing capacitor value = 0.1μF
R_T = Timing resistor value = 100kΩ

Therefore $\frac{dV_C}{dT_{mono}} = \frac{2.2}{0.1\mu F \times 100k} = 220V/s$

For $t_{mono(min)}$ = 1.0ms
$V_{C1} = 220 \times 1.0ms = 0.22V$

For $t_{mono(max)}$ = 2.0ms
$V_{C2} = 220 \times 2.0ms = 0.44V$

Therefore voltage across R_P = 0.22V

Therefore I = $0.22/R_P = 0.22/2k\Omega = 0.11mA$
$R_1 = V_{C1}/I = 2k\Omega$
$R_2 = 2.2 - V_{C2}/I = 16k\Omega$

For further information on the Monostable Timings refer to Section 1(e).

The circuit can be used over a wide range of supply voltages. In most cases it will only be necessary to change the base drive resistors R_{20}, R_{21} to ensure that there is sufficient base current to drive the output transistors into saturation under stall conditions. The value of the velocity feedback resistor RV_3 may also require adjustment.

Notes on Setting up the ZN409 Servo Board

1. RV_1, R_1, RV_2 and R_2 in conjunction with the Servo Potentiometer R_P determine the operating range of the servo (see Note 1(e)). The board is set up from an approximate range of 270° with an input pulse width of 1.5ms ± 0.5ms and a value of servo potentiometer R_P of 2.5kΩ. The pots RV_1 and RV_2 are to some extent interdependent, however, RV_1 will predominantly affect the servo range with 1.0ms input and RV_2 will affect the range at the 2.0ms input end.

2. RV_4 adjusts the pulse expansion characteristic (see Note 1(d)) which sets the gain of the system. A high gain (RV_4 set fully clockwise) will produce a fast response of the servo output but may result in instability, hunting and overshoot.

3. RV_3 adjusts the velocity feedback from the servo motor (see Note 1(f)).

Too low a value, (RV_3 set fully counterclockwise) will result in sluggish response close to the set point of the servo output. Too high a value of feedback resistance (RV_3 set clockwise) will produce overshoot and instability around the set point.

4. RV_5 adjusts the minimum output pulse width (see Note 1(e)). In the standard servo circuit this is fixed at 3.5ms but in this circuit it is variable down to <1ms. The minimum pulse width should be just sufficient to overcome the static friction in the output drive.

With the pulse width too small (RV_5 set fully counterclockwise) the servo will tend to undershoot and creep up to the set position. Too large a pulse width, (RV_5 fully clockwise) will produce 'cogging' and may also cause hunting and instability.

RESISTORS

All ¼W 2 %TOL unless stated)

R1	See text (1.6k)
R2	See text (12k)
R3	1M
R4	47k
R5	1k
R6	100k ½W High Stab 1% TOL
R7	1.2k
R8	47k
R9	10k
R10, R11	2.2k
R12, R13	1.2k
R14 to R19	10k
R20, R21	220 2.5W, 5% TOL
R22 to R25	22k
RV1	See text (1k)
RV2	See text (10k)
RV3	1M
RV4	100k
RV5	22k
RP	Servo Potentiometer (see text)

DIODES

D1, D2	1N4148

CAPACITORS

C1	220µF Electrolytic
C2	100µF Electrolytic
C3	0.22µF Tant
C4	2.2µF Tant
C5	1µF Tant
C6	100nF Ceramic
C7	100nF Polycarbonate
C8	4.7µF Tant
C9	47nF Polyester
C10	1000pF Ceramic

ICs

IC1	ZN409CE
IC2	LN340T5

TRANSISTORS

TR1, TR2	ZTX550
TR3, TR4	ZTX450
TR5, TR6	BUY82
TR7, TR8	BUY92
TR9	ZTX314

Table 3 Component list for ZN409 servo board

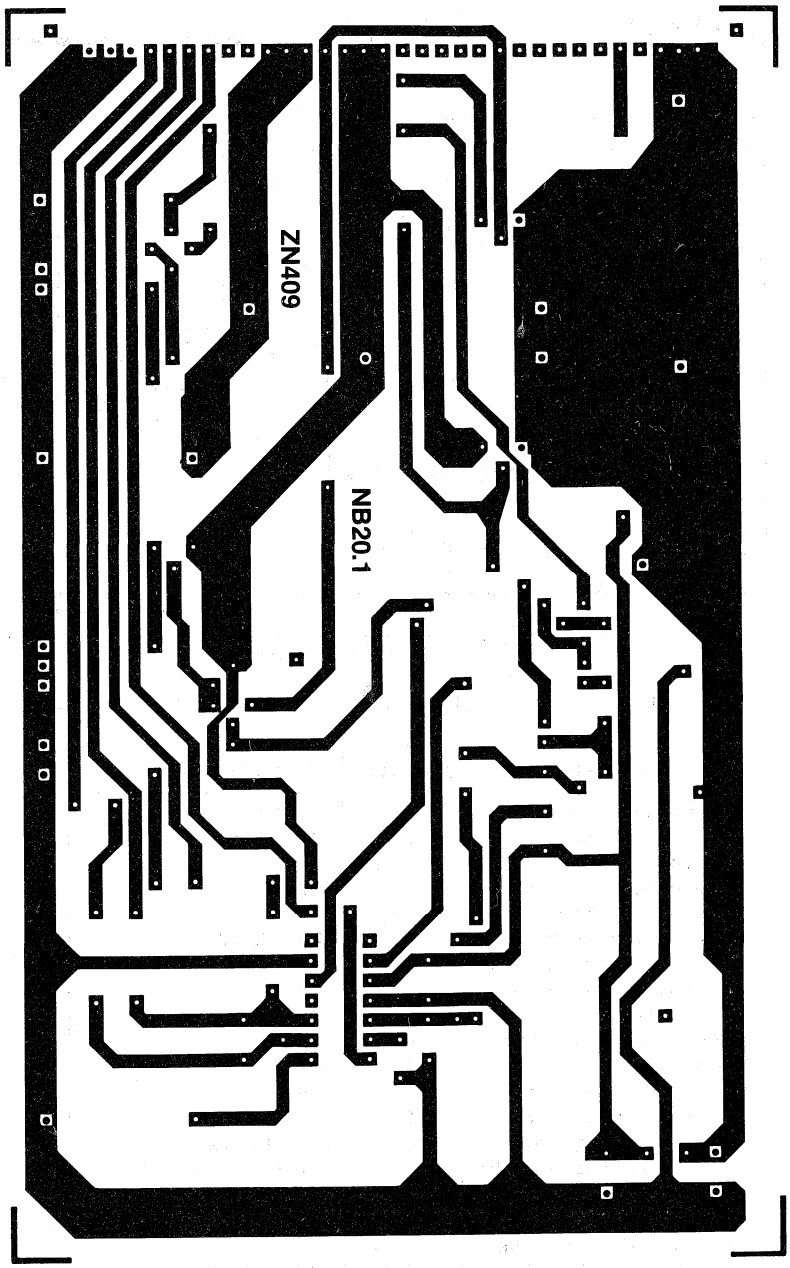


Fig.12

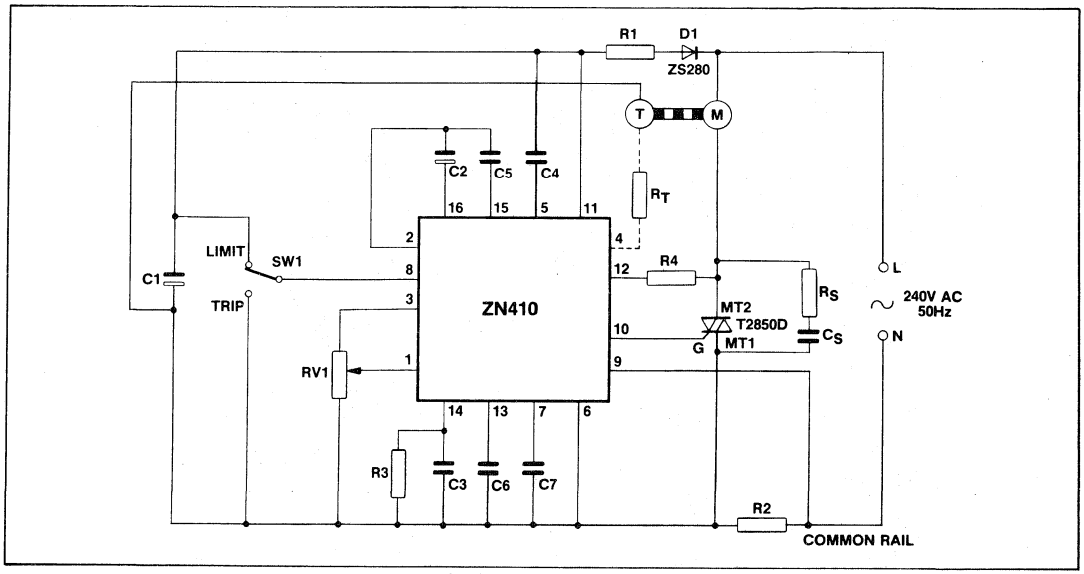


Fig.1 Reference system circuit diagram

NOTE: Component reference numbers apply to those shown on reference system circuit diagram, Fig.1.

Component function	Circuit ref.	Typical value
Supply dropper resistor	R_1	15k 3W
Current limit resistor	R_2	100mΩ (Note 1)
Tacho filter resistor	R_3	180kΩ
Current sync sense resistor	R_4	300kΩ
Tacho limit resistor	R_T	10kΩ
Triac snubber resistor	R_S	100Ω (Note 2)
Supply decoupling capacitor	C_1	100μF
Soft start ramp capacitor	C_2	10μF
Tacho filter capacitor	C_3	10nF
Tacho monostable capacitor	C_4	1500pF
Amplifier	C_5	0.47μF
Timing ramp capacitor	C_6	0.68μF
Current limit integrator	C_7	10μF
Triac snubber capacitor	C_S	0.1μF, 400V AC (Note 2)
Speed control potentiometer	RV_1	100kΩ

Table 1 Typical component values for Fig.1

NOTES

1. This value gives a current limit of 4A average.
2. Values are dependent on load and triac characteristics.
3. Triac type is dependent on load parameters.
4. Component values given are typical for a universal motor with characteristics of:

Power	750W
Maximum armature speed	30000 rpm
Tacho	Coil pick up with 6 pole pair rotor

5. Value of resistor R_T is dependent on tacho characteristics, to limit current to ≤2mA peak.
6. Switch SW_1 is optional and allows selection of limit or trip operation modes for current limit.
7. Positive supply pin 6 is connected as common.
8. The triac gate pulses are negative.

POWER SUPPLY OPTIONS

The ZN410 low cost motor speed controller incorporates a 5V nominal shunt regulator which supplies all the on-chip circuitry. External circuitry requiring a 5V supply can also be tapped off the IC supply pins as long as the IC current consumption requirements are satisfied.

In addition to the IC supply current on the specified data sheet, in the DC Characteristics, current must also be provided for the drive to the triac gate. Hence:

$$I_S = I_{CC} + I_{GT}\,(av)$$

Now the average value of the gate drive current will be:

$$I_{GT}\,(av) = I_{GT} \times t_{OUT} \times 2 \times f$$

where I_{GT} = Triac gate drive current
t_{OUT} = Triac gate drive pulse width
f = Mains supply frequency

Substituting some values:

Let I_{CC} (min) = 3.5mA
I_{GT} (max) = 130mA
t_{OUT} (max) = 150μs
f = 50Hz

Then I_S (min) $= 3.5 \times 10^{-3} + (130 \times 0.15 \times 10^{-6} \times 2 \times 50)$
$= 5.45$mA

The simplest supply option is shown in Fig.2.

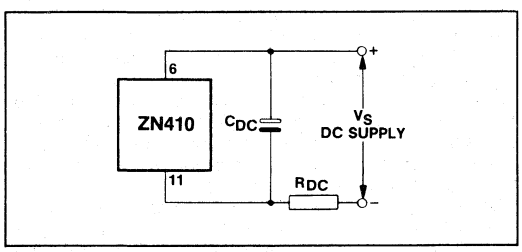


Fig.2 DC supply circuit

This can be used if a convenient DC supply is available. Note that the IC positive rail is normally the AC common (neutral) line. This circuit will function with a DC supply down to 6.5V.

The value of R_{DC} is given by:

$$R_{DC} = \frac{V_S - V_{CC}}{I_{CC}}$$

If V_S = 6.5V (min)
V_{CC} = 5.6V (max)
I_{CC} = 5.45mA (min)

Then $R_{DC} = \dfrac{6.5 - 5.6}{5.45} = 165\Omega$, say 160Ω

Taking 25mA as I_{CC} (max) then the maximum value of V_S is:

V_S (max) $= I_{CC}$ (max) $\times R_{DC} + V_{CC}$ (min)
$= 25 \times 10^{-3} \times 160 + 4.7$
$= 8.7$V

The main function of the capacitor C_{DC}, in addition to acting as a general decoupling capacitor is to absorb the triac gate current pulse. The capacitor value should be large enough to ensure that the drop in V_{CC} is less than 500mV, worst case. If V_{CC} drops more than this value there is a danger that the on-chip Power On Reset may be triggered, causing the circuit to malfunction.

The charge taken from capacitor C_{DC} is calculated as follows:

$$Q = C_{DC} \times v \text{ where } v \geqslant 500\text{mV}$$

Now $Q = I_{GT} \times t_{OUT}$

Therefore $C_{DC} \geqslant I_{GT} \times t_{OUT}/v$

i.e. Let I_{GT} = 130mA (max)
t_{OUT} = 150μs (max)

Then $C_{DC} > 130 \times 10^{-3} \times 150 \times 10^{-3} = 39\mu$F

Hence make $C_{DC} = 47\mu$F

The most useful method of powering the IC will be to supply it directly from the mains supply via a diode and resistive dropper, as shown in Fig.3.

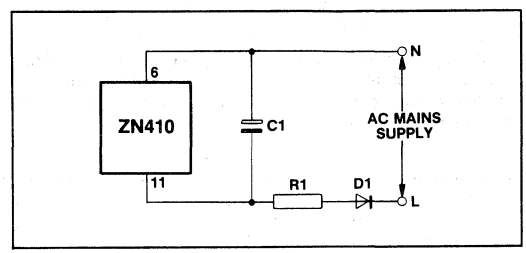


Fig.3 Mains supply via resistive dropper

With this configuration, current will only flow through the rectifier diode on negative half cycles of the AC supply. Assuming that the AC supply is much greater than the V_{CC} of the IC, then the value of R_1 approximates to the following formula:

$$R_1 = \frac{1.414 \times V_{AC}}{P_i \times I_S}\,\Omega \qquad \ldots (1)$$

Where V_{AC} = the RMS value of the AC supply.

Assuming a 240V ± 10% AC supply and a value of 5.45mA (min) for I_S, as found in the previous example, then:

$$R_1 \leqslant \frac{1.414 \times (240 - 10\%)}{P_i \times 5.45 \times 10^{-3}}$$

$R_1 \leqslant$ 17.84kΩ, say 15kΩ

The power dissipation in the dropper resistor is approximately:

$$P_{R1} = \frac{I_S\, P_i}{2} \times R_1 \text{ watts} \qquad \ldots (2)$$

Substituting for I_S from (1) gives:

$$P_{R1} = \frac{V^2_{AC}}{2R_1} \text{ watts}$$

To find the maximum dissipation with a value of R_1 = 15kΩ and a 240 ± 10% supply:

$$P_{R1}\,(max) = \frac{(240 + 10\%)^2}{2 \times 15 \times 10^3} = 2.32\text{W}$$

Hence a dropper resistor of 15kΩ, rated at 2.5W would be suitable with a 240V mains supply.

The decoupling capacitor in this circuit not only has to absorb the triac gate pulse but it must also supply the IC during the half cycle when the diode is not conducting. The total charge taken from C_1 during the non-conducting cycle is:

$$Q_T = Q_{GT} + Q_{CC}$$

Where $Q_{GT} = I_{GT} \times t_{OUT}$

And $$Q_{CC} = \frac{I_{CC}}{2f}$$

where f = frequency of the AC.
Substituting values of:

I_{GT} = 130mA
t_{OUT} = 150μs
I_{CC} = 3.5mA
f = 50Hz

Gives Q_T = 54.5μC

Now as before $\frac{Q_T}{C_1} < 500mV$

Therefore $$\frac{C_1 < Q_T}{500 \times 10^{-3}} < \frac{54.5 \times 10^{-6}}{500 \times 10^{-3}} < 109\mu F$$

For applications where a large value of decoupling capacitor is undesirable, or when additional circuitry is supplied from the IC shunt regulator a 2-stage filter circuit can be used as shown in Fig.4.

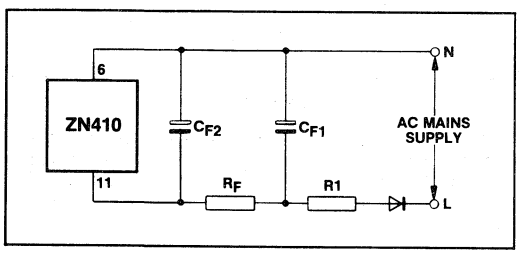


Fig.4 Mains supply with 2-stage filter

In this case R_F is chosen to drop 10V to 20V and the value of C_{F1} determines the level of ripple at the junction of C_{F1} R_F. A good approximation is to make the time constant C_{F1} R_F $\geq$ 30ms for 50Hz mains, using the previous value of I_S = 5.45mA are:

R_1 = 15kΩ, 2.5W
R_F = 2.4kΩ, 0.25W
C_{F1} = 22μF, 25V DC
C_{F2} = 47μF, 6.3V DC

Instead of a resistive dropper, a reactive dropper can be used, the advantage being that ther is negligible thermal dissipation in the reactive component. A circuit is shown in Fig.5.

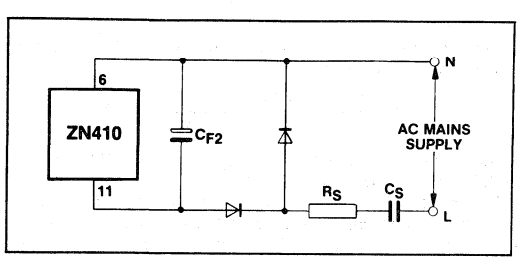


Fig.5 Mains supply with reactive dropper

The value of the reactive dropper capacitor C_S is given by the following expression:

$$C_S = \frac{I_S}{2\sqrt{2} \times V_{AC} \times f}$$

Substituting values of I_S = 5.45mA
V_{AC} = 240V
f = 50Hz

$$C_S = \frac{5.45 \times 10^{-3}}{2 \times 1.414 \times 240 \times 50}$$

$$= 0.16\mu F$$

Nearest preferred value = 0.22μF

The value of C_{F2} will be the same as the previous example, i.e. 47μF.

Resistor R_S is included to limit the surge current at switch on. A value of 330Ω is generally recommended for 240V operation, to limit the surge current to approximately 1A (max).

SPEED INPUT AND SOFT START

The ZN410 was designed to avoid the use of trimmer or 'select-on-test' components on the assembly line of the finished product. This is achieved by means of an on-chip voltage reference which supplies those parts of the circuit that have an influence on the speed calibration. This voltage is a band-gap reference which is buffered and appears on pin 3 as the Speed Reference Voltage. The IC is designed to be used with a 100kΩ potentiometer for the speed control connected between pin 3 and the positive supply pin 6. Minimum (zero) speed corresponds to the pin 6 end of the pot and maximum speed to the pin 3 end. The value of the pot itself is not very critical as long as the Speed Reference Input Current of 25μA is not exceeded; however for optimum matching a 100kΩ pot should be used.

Certain applications may require a control voltage to be fed directly to the Speed Input, pin 1. This is permissible, but for best speed calibration between devices the input voltage should be referenced back to the Speed Reference Voltage on pin 3. Note that both voltages are with respect to the positive rail pin 6, and pin 3 should not be left open-circuit, even if it is not used, connect it to pin 6 via a 100kΩ resistor.

The Soft Start function can be controlled by the value of capacitor across pins 2 and 16. When power is first applied to the ZN410 the Power On Reset circuit discharges this capacitor. It is then charged with a current of 8μA (typ) constant current to a level depending upon the setting of the speed control potentiometer. This will produce a linear rate of change of phase angle and hence approximate constant acceleration of the motor up to the set speed. The time constant from zero to full speed is given by the equation:

$$t_{SS} = \frac{C_2}{6} \text{ seconds, where C is in } \mu F$$

TACHO INPUT

The tacho input has been designed for use with a magnetic coil pickup, but this does not preclude the use of other types of tacho signals as long as the signal is interfaced correctly to the IC. The tacho input, pin 4, has a threshold centred around pin 6 as specified under the DC Characteristics. This input has bi-directional clamp diodes to pin 6 which allow the tacho pickup coil to be connected directly to pin 4, provided that the coil series resistance is sufficiently high enough to limit the input current to $<\pm$2mA. If not then an external resistor can be connected in series with the pickup coil. The front end of the tacho input circuit is shown in Fig.6.

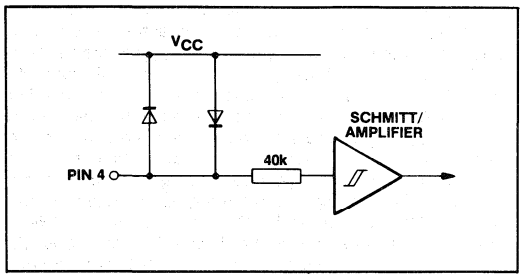


Fig.6 Tacho input circuit

The output of the Schmitt amplifier drives a charge dump circuit which transfers a constant charge from the capacitor on pin 5 (C_4), to the integrator R_C on pin 14 for each cycle of the taal. The voltage on pin 14 (w.r.t. pin 6), should equal the speed input voltage on pin 1 under conditions of equilibrium, i.e. speed constant. The speed control range can be calculated as follows:

If N = Armature speed (rpm)

and P = number of pole pairs of tacho

$$\text{Then tacho frequency} = \frac{NP}{60} \text{ Hz}$$

The voltage on the charge dump capacitor C_4 is equal to the Speed Reference Voltage (V_{SR}), i.e. 1.33V typ.

Hence the charge transferred per tacho cycle $= 1.33 \times C_4$

Therefore the average current flow through the integrator resistor R_3 on pin 14 is:

$$i = C_4 \times V_{SR} \times f_T$$

And the average voltage will be:

$$V_{(14)} = i \times R_3 = C_4 \times V_{SR} \times f_T \times R_3$$

Therefore for maximum speed the voltage on pin 14 should equal the maximum speed input voltage on pin 1, which is V_{SR}.

Hence $V_{SR} = C_4 \times V_{SR} \times f_T\,(max) \times R_3$

Therefore

$$f_T\,(max) = \frac{1}{C_4 R_3}$$

Or

$$N\,(max) = \frac{60}{C_4 R_3 P}$$

For example:

The nominal value of R_3 should be of the order of 100kΩ.

For a motor with an armature speed of 30000 rpm, and a 10 pole tacho:

$$N\,(max) = \frac{60}{C_4 R_3 P}$$

$$30000 = \frac{60}{C_4 \times 100 \times 10^3 \times 10}$$

$$C_4 = 2nF$$

A digital signal such as that from an Hall Effect tacho IC or other TTL type signal can be connected to the Tacho Input as shown in Fig.7.

The value of the capacitor is determined by the minimum input frequency, and the resistor limits the input current to $<\pm 2mA$ (max). Typical values for a TTL input would be:

$$C = 0.1\mu F,\ R = 4.7k\Omega$$

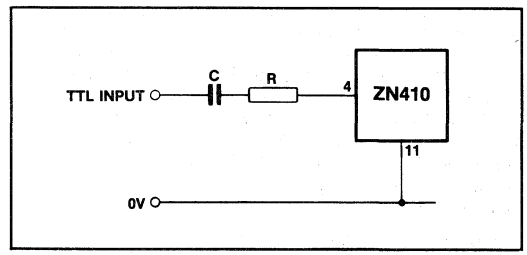


Fig.7 Tacho digital input

If the feedback signal is an analog voltage level then the f/V circuit can be bypassed and the signal fed to the Tacho Integrator pin 14 via suitable interfacing circuit. The operating range at this pin is from 0V to $-V_{SR}$ (−1.33V) w.r.t. pin 6. When used in this mode it is recommended that pin 4 is connected to pin 11 via a 10kΩ resistor, and pin 5 is let open circuit. Also the Tacho Integrator resistor R_3 and capacitor C_3, and Amplifier Filter capacitor C_5 will not normally be used.

ERROR AMPLIFIER

The function of capacitor C_3 on pin 14 is to integrate the current pulses through the resistor to produce a smooth DC level at pin 14 which is the non-inverting input of the Error Amplifier. Any remaining ripple is further filtered by an internal 50kΩ resistor and the capacitor C_5 connected between pins 15 and 2. It is not possible to specify values for these components since they will be dependent on various factors such as the dynamic characteristics and mechanical inertia of the motor and mechanical load, speed range required, number of tacho poles used, etc. Usually these values will have to be found empirically, but as a general guide the following points can be used for guidance.

1. The time constant on pin 14 (i.e. $C_3 R_3$) will normally be in the range 1 to 20ms. If this time constant is too large it will cause instability problems especially on load. At the other end of the range, the slow running performance of the motor will be degraded if the time constant is too small. A second factor to consider is that the ripple amplitude does not drive the amplifier input beyond its common mode range of 0V to −1.65V (w.r.t. pin 6).

2. The time constant on pin 15, (i.e. $C_5 \times 50k\Omega$), will normally be in the range 20 to 200ms. If this value is too large it can cause instability resulting in overshoot with changing loads and at switch on. Again, too small a value results in poor low speed performance of the motor, but this is more critical than the time constant of pin 14.

A general rule for low speed performance, especially for low inertia motors is: use a tacho with as high a number of poles as possible.

The Error Amplifier is a fixed gain circuit which compares the Speed Input voltage with the voltage on pin 14 proportional to the tacho frequency. Any difference is amplified and the output level is compared against a reference time ramp, to determine the firing point of the triac with reference to the start of the mains cycle.

RAMP GENERATOR

The Ramp Generator produces a negative going ramp voltage which is synchronised to the AC mains waveform and starts at the beginning of each cycle. This ramp voltage is applied to one input of a comparator. The other input is driven from the Error Amplifier output. The point at which the

ramp voltage crosses the amplifier output level determines the point in the mains cycle at which the triac is gated on. Hence the ramp acts as a timing reference - if the error amp output goes more negative the triac fires later in the cycle, reducing the power to load, and vice-versa.

The ramp voltage is generated by a current source charging an external capacitor C_6 on pin 13. The value of this capacitor can be calculated as follows:

Normal maximum negative excursion on pin 13 = -1.45V (w.r.t. pin 6).

Ramp discharge voltage = -0.75V

Charge voltage across capacitor V_{C6} = 0.7V

Now $$V_{C6} = \frac{I}{2f \times C_6}$$ where F = mains frequency, I = charge current

Hence $$C_6 = \frac{I}{2f \times V_{C6}} = \frac{0.7I}{f}$$

For example: if f = 50Hz, I = 50μA (typ.)

Then $$C_6 = \frac{0.7 \times 50 \times 10^{-6}}{5} \quad 0.7\mu F$$

Nearest preferred value = 0.68μF.

Some control over the overall gain of the system can be achieved by changing the amplitude of the ramp voltage through a different value capacitor. However the ramp voltage should not be made too small (corresponding to a high system gain) otherwise instability may result. Also care should be taken to limit the maximum negative peak of the ramp to -2.5V (w.r.t. pin 6) under worst case conditions, otherwise it will exceed the output range of the Error Amplifier causing malfunction of the IC.

SYNCHRONISATION

The function of the Sync Input, pin 12, is to discharge the ramp capacitor when the mains cycle crosses zero. Normally two sync inputs would be used, one to detect the zero on the mains voltage waveform and discharge the ramp capacitor, and a second current syn which delays the firing of the triac until the load current has fallen to zero and the triac turned off from the previous half cycle. This is necessary, in order to achieve high conduction angles when driving inductive loads.

The ZN410 differs from standard practice, in having only one sync input, which essentially is a current sync. The benefit of this is that it saves on external components and package pins, thereby saving on costs. In use the Sync Input, pin 12, is connected via a resistor to a point between the MT2 terminal of the triac and the load. When the triac is conducting the voltage across it is only 1 to 2V and negligible current flows in the Sync Input. At the end of the half cycle, when the load current falls below the holding current the triac will turn off and as the voltage increases on the next half cycle the current flowing in the input will increase. When the current exceeds the threshold current the Ramp capacitor discharge transistor is switched off allowing the timing ramp to start. At the point in the cycle when the triac fires the current flowing in pin 12 will fall back below the threshold and the discharge transistor will switch on discharging the Ramp capacitor C_6 ready for the next half cycle. The value of resistor connected to pin 12 sets the mains voltage level at which the timing ramp starts. This point will correspond to the earliest point in the cycle at which the triac can be switched on. Normally the resistor is selected so that the mains voltage, at this point, will be sufficient to produce a load current through the triac and load greater than the specified triac latching current. Usually this would be between 25 and 50V (Note - 50V corresponds to a conduction angle of >170 degrees).

A potential disadvantage of using only one sync input on the ZN410 is that it is not possible to guarantee that under all conditions, a triac retrigger pulse will be generated should the triac somehow turn itself off part way through its conduction cycle. In practice this rarely happens provided that the triac is operated within its specification of gate pulse width, gate current and latching current. Usually, on the occasion when it does happen, it is under conditions of full drive, at a point in the cycle when the mains voltage is low and hence the latching current marginal. However, under these conditions, close to the start of the cycle, the ZN410 will generate retrigger pulses shortly after the triac drops out, it is only if drop-out occurs later in the cycle that a retrigger pulse will not be generated.

TRIAC OUTPUT

The Triac Gate Output circuit produces constant current negative going pulses, for more balanced firing of the triac, and allows direct connection of the output to the gate terminal of the triac. The gate current level and pulse width are preset internally in the ZN410 and are suitable for most small to medium power triacs. The maximum gate current can be limited by means of an external resistor. The only advantage of this would be when using a sensitive gate triac, the supply current to the ZN410 could be decreased, to allow the Shunt Regulator dropper resistor R_1 wattage and capacitor C_1 size to be reduced, since the normal gate current constitutes more than 30% of the device supply current. The value of an external limiting resistor can be calculated from:

$$R_L = \frac{4.7 - V_{GT}}{I_{GT}} - 10\Omega$$

where V_{GT} is the triac gate voltage, and I_{GT} is the required gate current in Amperes.

CURRENT LIMIT/TRIP

The voltage applied to the Current Limit Input, pin 9, is integrated and compared against a preset level by a comparator. The circuit is designed to operate in two modes, controlled by the state of the Limit/Trip Switch Input, pin 8. With this switched to pin 11 the comparator output is used to discharge the Soft Start capacitor C_2, thereby reducing the triac conduction angle and hence average load current until the input voltage falls below the preset limit. This level corresponds to a mean voltage at the input of 425mV, which is equivalent to 4.7A RMS through a 100mΩ resistor. This sense resistor R_2 is usually connected in series with the load, normally between V_{CC} pin 6 and the Neutral line as shown in Fig.1. Note that if the transient load current is likely to produce in excess of 5V peak across the sense resistor then a limiting resistor of the order of 10kΩ should be connected in series with the input pin 9 to protect the IC from damage. The time constant of the integrator formed between the Limit capacitor C_7 on pin 7 and an internal 150kΩ resistor should be selected to be of the order of tens of mains cycles. A high value will result in a slow response of the circuit to an overload, whereas a low value will produce a fast response, but as the integrator time constant is reduced the circuit will react more to the peak rather than the average value of the load current. This will result in foldback of the Speed/Torque characteristic, which may be a useful feature for certain applications.

When pin 8 is connected to 0V (pin 6) the circuit operates as a current trip function. As soon as an overload condition causes the integrated voltage to exceed the preset level a latch is set which inhibits the output drive to the triac. This latch is only reset by the action of the Power On Reset, so the supply to the ZN410 has to be switched off and on again to re-establish the output drive.

Note that the Current Limit function should be used as a torque limiting mechanism rather than an overload protection for the motor. This is due to the fact that most universal motors rely on a centrifugal fan for cooling, the efficiency of which deteriorates considerably at low speed causing rapid overheating of the motor. If overload protection is required then the Current Trip function is recommended.

VARIABLE CURRENT LIMIT

A method of implementing an adjustable current limit is shown in Fig.8. A potentiometer, RV_1, is connected in parallel with the normal sense resistor R_2. The value of the pot is not critical; any value in the range 100Ω to 10kΩ will be suitable. The value of R_2 is calculated for the minimum value of current limit. With the pot wiper at pin 6 end the current limit is infinite, whereas at the opposite end it is as determined by the value of R_2. Note that care should be taken to ensure that the peak voltage across R_2 does not exceed ±5V, otherwise a limiting resistor needs to be connected in series with the Current Limit input pin 9.

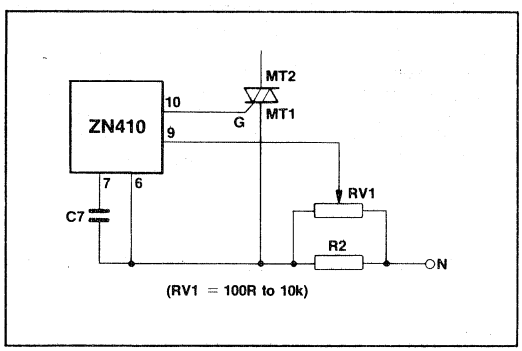


Fig.8 Variable current limit

DRIVING HIGH POWER TRIACS

A method of driving high power triacs which requires a gate current in excess of that supplied directly from the Triac Gate Drive output pin 10 is shown in Fig.9. An external PNP transistor is used as an emitter follower with the base driven from the Triac Drive output, with a pull up resistor to the +Vcc pin 6. The value of emitter resistor can be calculated from:

$$R_G = \frac{4.1 - V_{GT}}{I_{GT}}$$

where I_{GT} = gate current required
V_{GT} = gate voltage at specified I_{GT}.

Note that allowance must be made for the gate current when calculating R_1 and C_1 as explained previously.

OPTICAL TACHO INPUT

Fig.10 illustrates a typical circuit for use with an opto-switch to measure the motor speed instead of a magnetic pickup. The component values may have to be changed from those shown, dependent upon the motor speed and number of slots used in the rotating shutter. The signal level on the Tacho input pin 4 of the ZN410 should be >±100mV w.r.t. the Vcc pin 6. Rx should be calculated to limit the maximum input current on pin 4 to ±2mA.

Note that the opto-switch circuit is powered from the ZN410 supply, hence the current drawn by the circuit should be kept as low as possible. The value of the dropper resistor R_1 and decoupling capacitor C_1 are calculated to take account of this current. Also the Tacho Dump capacitor C_4 and Tacho Integrator resistor R_3 are selected as described under TACHO INPUT to match the tacho frequency.

i.e.

$$f_T\,(max) = \frac{1}{C_4 R_3}$$

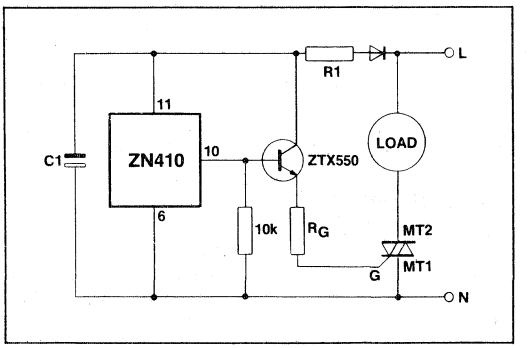


Fig.9 High gate current triac drive

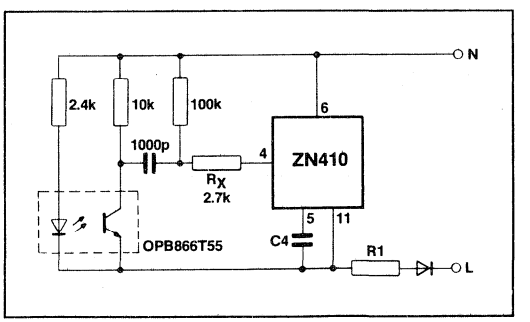


Fig.10 Opto-tacho circuit

OPEN LOOP PHASE CONTROL

The ZN410 can be used as an open loop phase controller simply by reducing the Speed Input voltage by a factor of approximately 6:1 and disabling the tacho circuit. This is shown in Fig.11. The ratio of the resistor values, R_A and R_B are selected to produce the required phase control range. Note the value of $R_A + R_B$ should be of the order of 100kΩ. The values shown will allow control over almost the full 180 degrees. The tacho circuit is disabled by leaving pins 4, 5, and 15 open circuit and connecting pin 14 to Vcc (pin 6). Although not shown in the diagram the soft start and current limit functions can be used with the open loop configuration.

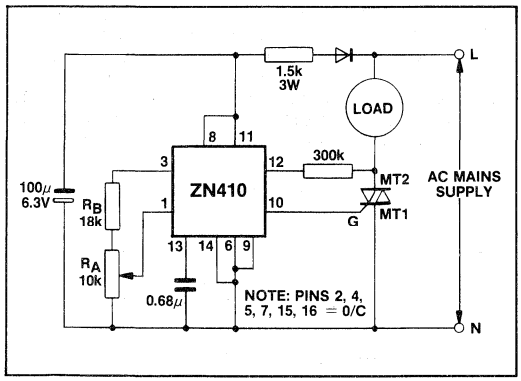


Fig.11 Open loop phase control circuit

VARIABLE RAMP CONTROL

The addition of a resistor between the Soft Start pin 2 and 0V pin 11 can be used to change the soft start ramp for applications such as washing machines etc. (see Fig.12). The normal Soft Start Ramp time constant is given by the equation:

$$t = \frac{8}{C_2} \text{ v/s } (C_2 \text{ in } \mu F)$$

i.e. The charging current $= 8.0\mu A$.

With the addition of a resistor R_C between pins 2 and 11 the time constant becomes approximately:

$$t = \frac{4000}{C_2 R_C} \text{ v/s } (C_2 \text{ in } \mu F, R_C \text{ in } k\Omega)$$

for values of $R_C \leqslant 200k\Omega$.

Hence for a 10:1 change in ramp time, $R_C = 56k\Omega$.

The main disadvantage of this method concerns the operation of the Soft Start capacitor C_2. If the positive end of C_2 is connected to pin 16, then switching in resistor R_C causes an immediate step in the speed due to the change in voltage across the internal diode as a result of the extra current flow, i.e. for $R_C = 56k\Omega$, this corresponds to a 10:1 change in current and hence 68mV change in voltage at pin 2 (p-n junction produces 68mV per decade of current change). The alternative is to connect the positive end of the capacitor to V_{CC} pin 6. However this results in an initial delay before the motor starts at switch-on from cold, since the capacitor has to charge up to at least V_{be} (0.7V). This may be acceptable for most applications. Also the advantage over the other method is that the capacitor discharges rapidly through the transistor as the speed input is reduced, whereas with it connected to pin 16 this discharge path is blocked by the diode, and hence the capacitor can only discharge through the $8.0\mu A$ current source. The effect of this is to limit the range over which the soft start will operate, if the speed input signal is reduce and then increased again shortly afterwards, before the capacitor has had time to fully discharge. The value of C_2 is recommended to be $\leqslant 100\mu F$ for this application.

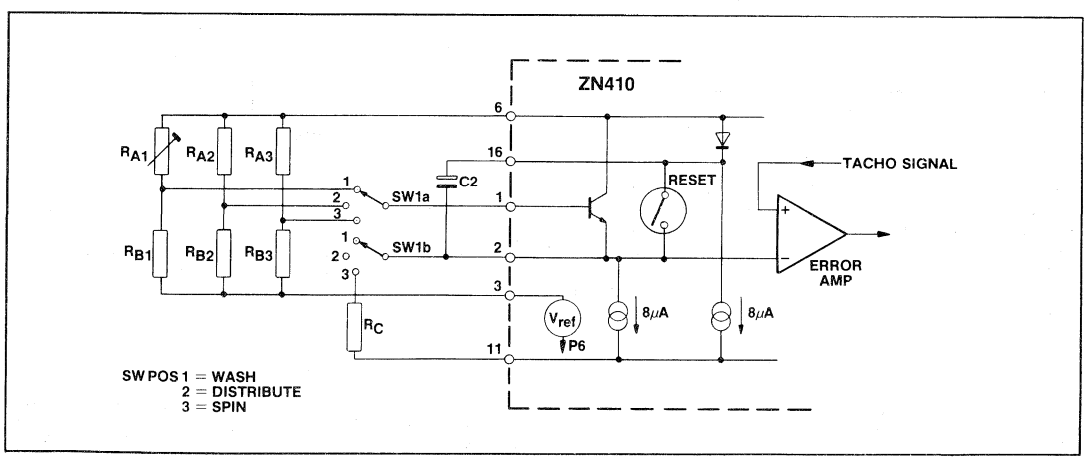


Fig.12 Variable ramp circuit

System Design with the ZN411

Throughout this section, component references are to those shown on Fig.1.

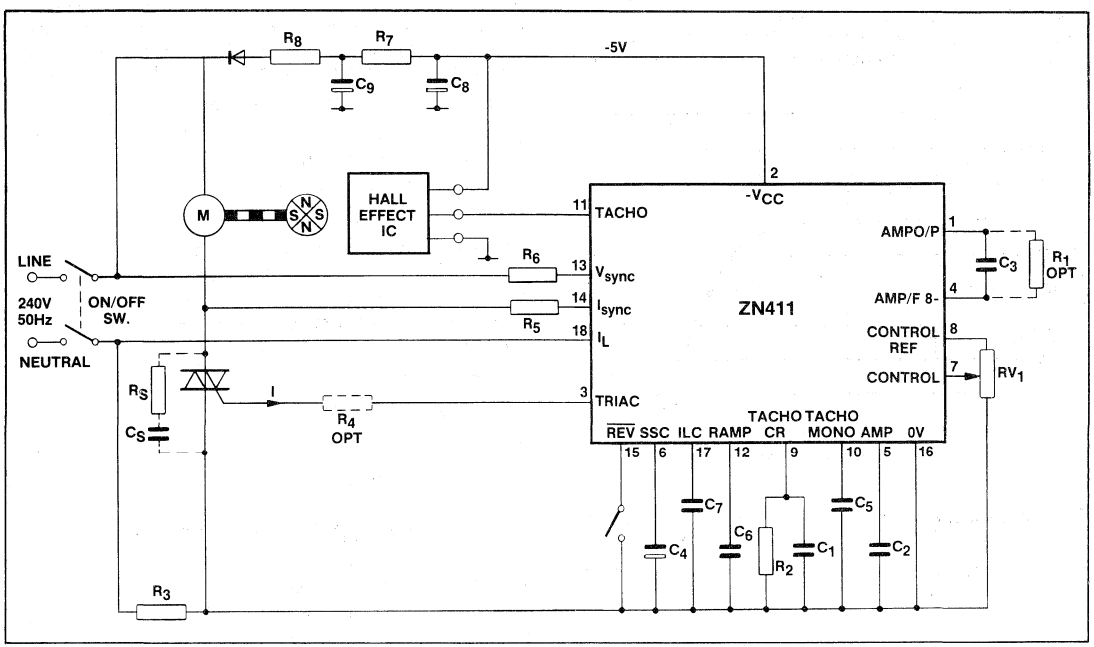


Fig.1 Reference system circuit diagram

Component Function	Circuit Ref.	Typical Value	Relevant Section(s)
Error amplifier gain resistor	R_1	infinity	5
Tacho integrator resistor	R_2	180kΩ	4
Current limit resistor	R_3	0.1Ω 2.5W	9
Triac gate current limit resistor	R_4	zero	8
Current sync sense resistor	R_5	270kΩ	7
Voltage sync sense resistor	R_6	330kΩ	7
Supply filter resistor	R_7	430Ω	2,8
Supply dropper resistor	R_8	5.6kΩ 4W	2
Tacho integrator capacitor	C_1	0.1μF	4,5
Tacho output filter capacitor	C_2	47nF	4,5
Dynamic response capacitor	C_3	0.22μF	5
Soft start ramp capacitor	C_4	10μF	3,5,9,10
Tacho monostable capacitor	C_5	6800pF	4
Timing ramp capacitor	C_6	0.1μF	6
Current limit integrator capacitor	C_7	0.47μF	9
Supply decoupling capacitor	C_8	22μF 6.3V	2,3
Supply filter capacitor	C_9	68μF 16V	2
Speed control potentiometer	RV_1	100kΩ	3

Table 1 Typical external component values

Fig.1 illustrates a circuit for a closed loop Universal Motor Speed Control. Feedback is provided by a 2-pole magnetic rotor connected directly to the motor armature which is sensed via an hall effect IC. A list of typical external component values is shown in Table 1 and a graph of speed/torque curves is shown in Fig.2. These were taken from a 400 watt motor driving a 10:1 ratio gearbox with a no load output shaft speed of 2800 rpm.

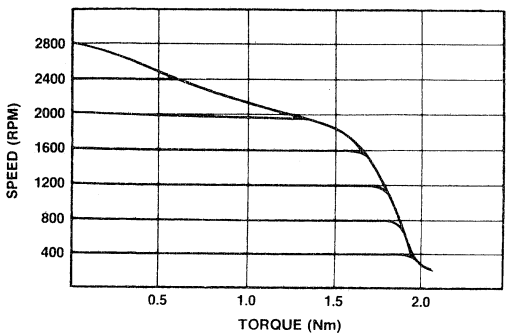


Fig.2 Speed/Torque curves

1. The component values can be found from the following formula (refer to Table 2 for Symbol Definitions):

Let total supply current $I_S = I_{CC} - I_{ext}$ where I_{ext} is the current taken by any additional external circuitry (i.e. Hall Effect Tacho device).

Initially we need to select a capacitor for C_9 with a maximum working voltage, V_{wkg} of normally 16V or 25V (with 240V mains supply).

$$\text{Now let } V_{1(max)} = V_{wkg} - 20\% \qquad \ldots (1)$$

to allow for mains voltage variation etc.

In order to keep the ripple voltage, V_r on C_9 down to an acceptable level, make the time constant

$$C_9 R_7 \geqslant 30\text{ms} \qquad \ldots (2)$$

Since the voltage supplied to C_9 is half wave rectified the ripple voltage will be:

$V_r = I_S \times 10\text{ms}/C_9$ V p-p

Substituting in Eq. (2) gives:

$$V_r \leqslant 0.33\, I_S R_7 \text{ V p-p} \qquad \ldots (3)$$

Now

$$R_7 = \frac{V_1 - V_S}{I_S}$$

and since the mean value of $V_1 = V_{1(max)} - \frac{1}{2}V_r$

Then

$$R_7 = \frac{V_{1(max)} - \frac{1}{2}V_r - V_S\Omega}{I_S} \qquad \ldots (4)$$

where V_S = Shunt regulator voltage (5.1V typical)

Substituting for R_7 in Eq. (3) gives:

$$V_r \triangleq 0.3(V_{1(max)} - V_S)\text{V p-p} \qquad \ldots (5)$$

If the voltage V_1 on C_9 is made much less than the AC supply voltage, (say $\leqslant 10\%$ of V_{AC} (rms)), then the value of R_8 approximates to:

$$R_8 \triangleq \frac{\sqrt{2} \times V_{AC} - V_1}{\pi \times I_S} \qquad \ldots (6)$$

where V_{AC} is the rms value of the mains supply.

The power dissipation in R_8 also approximates to:

$$P_d = \left[\frac{I_{S(max)} \times \pi}{2}\right]^2 \times R_8 \text{ watts} \qquad \ldots (7)$$

The function of capacitor C_8 is to maintain the ZN411 supply voltage at a value above the switch-on reset level during the triac gate pulse period. C_8 should be chosen so that the voltage drop during the pulse period is $\leqslant 0.5$V.

Hence

$$C_8 \geqslant I_G \times t_G/\delta V_S$$
$$\geqslant 2(I_G \times t_G)\ \mu\text{F} \qquad \ldots (8)$$

where I_G = Gate output current (mA)
t_G = Gate output pulse width (ms)

To consider an example:

Let maximum supply current I_S = 8mA
Mains voltage V_{AC} = 240V rms
ZN411 supply voltage V_S = 5.1V
Let V_{wkg} of C_9 = 25V DC working voltage
Then from Eq. (1) $V_{1(max)} = 25\text{V} - 20\% = 20\text{V}$

The ripple voltage on C_9 given by Eq. (5) is

$V_r = 0.3\ (20 - 5.1) = 4.4$V p-p

Now from Eq. (4)

$$R_7 = \frac{20 - \frac{1}{2} \times 4.47 - 5.1}{8\text{mA}}$$

$= 1583\Omega$, say $\underline{1.5\text{k}\Omega}$ (Nearest preferred value)

Now if $R_7 C_9 \geqslant 30\text{ms}$
Then $C_9 \geqslant 30\text{ms}/1.5\text{k} \geqslant 20\mu\text{F}$
Hence let $\underline{C_9 = 22\mu\text{F}}$
Now $V_{1(nom)} = V_{(max)} - \frac{1}{2}V_r$
$= 20 - \frac{1}{2} \times 4.47 = 17.7\text{V}$

From Eq. (6)

$$R_8 = \frac{\sqrt{2} \times 240 - 17.7}{\pi \times 8\text{mA}} = 12.8\text{k}\Omega$$

Hence let $\underline{R_8 = 12\text{k}\Omega}$

Now substituting R_8 back in Eq. (6) to find $I_{S(max)}$ gives

$$I_S = \frac{\sqrt{2}(240 + 10\%) - 17.7}{\pi \times 12{,}000}$$

$$\underline{I_{S(max)} = 9.43\text{mA}}$$

Therefore from Eq. (7) the maximum dissipation in R_8 will be:

$$P_d = \left[\frac{9.43\text{mA} \times \pi}{2}\right]^2 \times 12{,}000$$
$$= 2.63\text{W}$$

Let rating of $\underline{R_8 = 3\text{W}}$

Finally taking $I_{G(max)} = 140\text{mA}$
$t_{G(max)} = 150\mu\text{s}$

Then C_8, from Eq. (8)
$\geqslant 2(140\text{mA} \times 0.15\text{ms}) \quad \geqslant 42\mu\text{F}$
Let $\underline{C_8 = 47\mu\text{F (6.3V)}}$

In an actual design case the tolerances of the mains supply and components selected should be taken into account.

NOTE: A more accurate formula for R_7 is given by:

$$R_7 = \frac{0.668V_{wkg} - 4.26}{I_S}$$

2. POWER SUPPLY OPTIONS

The ZN411 contains an on chip 5V shunt regulator which allows the device supply to be generated by several different methods. The most convenient method will normally be to power the device from the AC mains supply, via a half wave rectifier diode and dropper resistor (R_8) as shown in Fig.3:

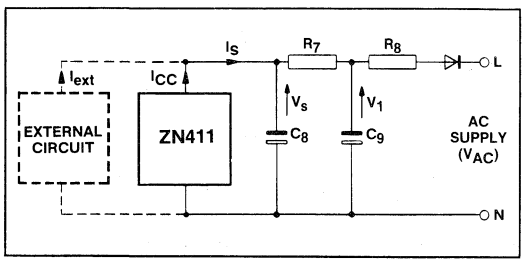


Fig.3 Power supply using diode and dropper resistor

The main disadvantage of using a dropper resistor is usually one of heat dissipation in the resistor. This can be overcome by using a reactive dropper circuit as shown in Fig.4:

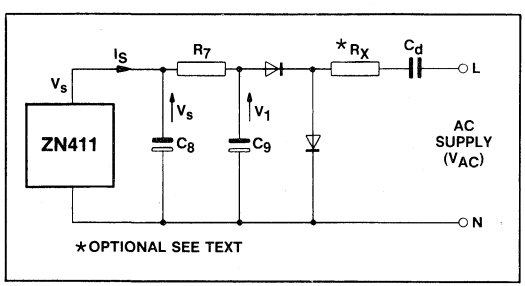


Fig.4 Power supply using reactive dropper circuit

In this case the component values are calculated as follows:

Neglecting diode volt drop, the charge transferred via capacitor C_d is given by:

$Q = C_d (2V_{pk} - V_1)$

Now $i = Q/t = Qf$ where f = mains frequency.

Therefore $i = C_d \times f (2V_{pk} - V_1)$

Now since $i = I_S$ and $V_{pk} = \sqrt{2}\, V_{AC}$

Then

$$C_d = \frac{I_S}{f (2.82\, V_{AC} - V_1)} \quad \ldots (9)$$

Resistor Rx can be included to limit the surge current at switch on. A value of 330Ω is generally recommended to limit the surge current to the order of 1 amp maximum.

Equations (1) to (5) for the selection of C_9 and R_7 and equation (8) for C_8 still apply for a reactive dropper circuit.

To consider an example, taking the same conditions as previously:

With $V_{1(nom)} = 17.7V$

$$C_d = \frac{I_S}{f (2.82\, V_{AC} - V_1)} = 8mA/50\ (2.82 \times 240 - 17.7)$$

$\underline{C_d = 0.24\mu F}$

Nearest preferred values are 0.22 and 0.33μF

Using a 0.22μF will give a supply current of

$I_S = C_d \times f (2.82\, V_{AC} - V_1)$

$= 0.22 \times 10^{-6} \times 50\ (2.82 \times 240 - 17.7)$

$I_S = 7.25mA$ (nominal)

If this is too low a 0.33μF capacitor will have to be used.

Substituting this value of C_d in Eq. (9) gives:

$I_S = 10.87mA$

With $R_7 = 1.5k\Omega$ as calculated in the previous example, the voltage V_1 from Eq. (4) will now be:

$V_{1(nom)} = R_7 \times I_S + V_S = 21.4V$

and since

$$V_r = \frac{I_S \times 10ms}{C_9}$$

$V_r = 4.93V$ p-p

Hence $V_{1(max)} = 21.4 + 4.93/2 = \underline{23.8V}$

This is rather close to the maximum DC working voltage of C_9 chosen previously of 25V, and it would be advisable to select a higher working voltage capacitor in the range of 35 to 40V.

This example illustrates a problem of using a capacitive dropper. It is not always easy to select a preferred value of C_d for the design characteristics required.

Alternatively the value of R_7 can be reduced to maintain the same value of V_1, and C_9 will have to be increased in value to comply with Eq. (2).

Operation from stabilised or unstabilised DC supplies is possible simply by using the following circuit.

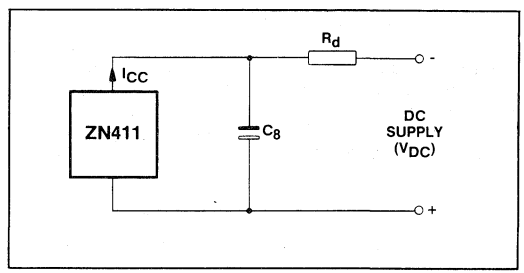


Fig.5 Operation from stabilised or unstabilised DC power supplies

The value of R_d can be found from:

$$R_d = \frac{V_{DC} - V_{CC}}{I_{CC}}$$

The value of C_8 will be the same as that calculated previously.

Note that when designing with unregulated supplies the value of the resistor (R_d) should be calculated by taking into consideration the minimum and maximum peak values of the supply. Where possible the DC supply should be made much greater than the shunt regulator voltage in order to keep the supply current within specification.

3. SPEED CONTROL AND SOFT START

The ZN411 has been specially designed so that for the majority of applications no production line adjustments are necessary and satisfactory calibration of the operating characteristics can usually be achieved by using fixed values for all external components. This built in calibration was designed around a number of accurately matched current sources which are used in the critical areas of the circuit that affect the speed calibration.

One of these current sources is connected to the Control Ref. pin 8, and sources a nominal current of 20 microamps through the Speed Control potentiometer. This develops a voltage of nominally 2.0V across the potentiometer, the value of which should be 100kΩ. The circuit was designed to use this particular value of potentiometer and use of a different value will limit the speed control range of the device. The voltage applied to the Control input pin 7 adjusts the conduction angle of the triac and hence the speed of the motor.

For certain applications other forms of speed control input, rather than a potentiometer may be necessary, (e.g. microprocessor control via a D/A converter). In these cases a fixed 100kΩ resistor should be connected from 0V to pin 8, and the control voltage applied to pin 7 should be referenced to the voltage at pin 8 (w.r.t. to 0V rail). Failure to do this will result in poorer performance over the temperature range, and in addition the system would probably have to be recalibrated if the ZN411 was changed.

The rate of rise of the control voltage applied to the Error Amplifier is governed by the Soft Start capacitor C_4. When power is first applied to the ZN411 the Switch-on Reset circuit ensures that this capacitor is fully discharged. A 10 microamp current source then charges the capacitor and the voltage on the capacitor rises linearly to a level determined by the setting of the speed control pot. Thus with a normal circuit the motor speed will rise at a constant rate (i.e. constant acceleration) until it reaches the preset level. The time for the capacitor to obtain full charge, with V pin 7 = V pin 8 (i.e. maximum speed) is given by the equation:

$$t_{ss} = C/5 \text{ secs} \qquad \ldots (10)$$

where C is the value of C_8 in microfarads.

Note that the charge rate is constant irrespective of the voltage applied to the control input, therefore with the control potentiometer set midway (i.e. Half full speed), the soft start time will be half of that calculation in Eq. (10). Also it should be borne in mind that the total time for the motor to attain the set speed will also be affected by mechanical considerations, such as the inertia of the system, and the load torque.

4. TACHO INPUT AND F-A CONVERTER

The Tacho input, pin 11 was designed primarily for use with Half Effect Switch IC's such as the UGN-3013T device, although magnetic coil pickups can also be used and are easily interfaced.

The input circuit on pin 11 is shown in Fig.7.

The open collector output of the Hall Effect Switch IC can be directly connected to pin 11 so that the internal 40kΩ resistor will act as a pull up resistor for the IC output. The 320kΩ input resistor and capacitor form a low pass filter to reject any hf noise spikes on the input.

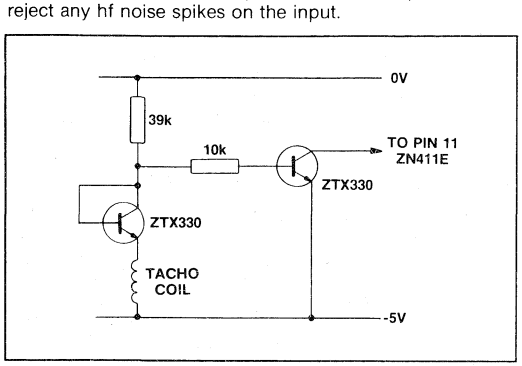


Fig.6 Magnetic coil pickup buffer

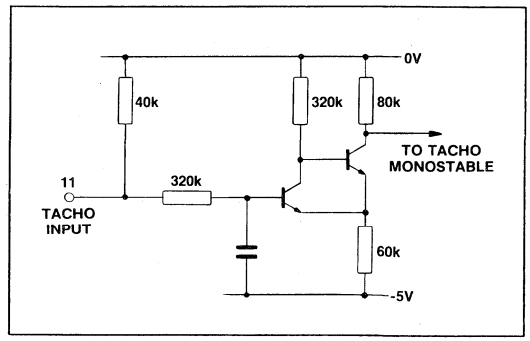


Fig.7 Input circuit on pin 11

The Tacho Monostable time is given by the equation:

$$t_{mono} = \frac{C_5 \times V_{ref}}{I_1} \text{ (sec)} \qquad \ldots (11)$$

where V_{ref} = Voltage at pin 8 (nominally 2.0V).
I_1 = 55μA, the value of the current source on pin 10.
C_5 = Capacitor connected across pins 10-16 (in microfarads).

t_{mono} must be less than the minimum period of the Tacho input.

Therefore $t_{mono} < 1/f_{T(max)} < \frac{60}{N_{(max)} \times P}$ (sec)

where $f_{T(max)}$ = Maximum tacho frequency.
$N_{(max)}$ = Maximum armature speed (rpm).
P = Number of poles on the tacho.

Substituting in Eq. (11).

$$\frac{C_5 \times V_{ref}}{I_1} < \frac{60}{N_{(max)} \times P}$$

Therefore $$C_5 < \frac{60 \times I_1}{V_{ref} \times N_{(max)} \times P} \qquad \ldots (12)$$

In order to allow for component and processing tolerances the nominal value of the monostable capacitor should be calculated from:

$$C_5 = \frac{500}{N_{(max)} \times P} \ \mu F \qquad \ldots (13)$$

The Tacho Monostable circuit gates constant current pulses to an RC integrator formed by C_1 and R_2 on pin 9. At maximum speed the voltage on pin 9 should be equal to the Control Bias voltage on pin 8.

Hence - V_{out} (pin 9) $= V_{ref} = I_{avg} \times R_2$
$= I_2 \times t_{mono} \times f_{T(max)} \times R_2$

Where I_2 = value of pulsed current source.

Substituting t_{mono} from Eq. (11).

$$V_{ref} = I_2 \times \frac{C_5 V_{ref}}{I_1} \times f_{T(max)} \times R_2$$

Now $I_2 = I_1$ (by design) and this equation simplifies to:

$$R_2 = 1/C_5 \times f_{T(max)} = \frac{60}{C_5 \times N_{(max)} \times P} \qquad \ldots (14)$$

The value of C_1 determines the tacho integration time constant and therefore the amplitude of the ripple on pin 9. The signal from pin 9 is buffered and fed to the non-inverting input of the Error Amplifier via a second stage of filtering comprising of an internal 160kΩ resistor and capacitor C_2 connected to pin 5. The amplitude of the ripple on the output of the Error Amplifier is then determined by the values of both C_1 and C_2 and also by the AC gain of the amplifier. This ripple voltage results in a slight variation of the firing angle of the triac but this is normally damped by the mechanical inertia of the motor and is usually undetectable. However, at low speed the ripple voltage can beat with the mains frequency to produce a low frequency speed variation in the drive.

The value of C_1 and C_2 can be increased in order to reduce the ripple and hence 'beating' effect. These capacitors also affect the dynamic response of the system and if they are too high sluggish response of the motor will result. In most systems satisfactory dynamic performance and low speed operation can usually be obtained by empirical selections of C_1 and C_2 in conjunction with C_3 as described in the next section. In extreme cases the tacho ripple voltage can always be reduced by using a tacho rotor with a larger number of poles.

As a general rule if low speed operation is required especially for motors with low mechanical inertia then it is good design practise to use a tacho with the maximum number of poles that cost and physical limitations will permit.

5. ERROR AMPLIFIER

The Error Amplifier was designed to have an open loop DC gain of typically 40 and a closed loop AC gain of typically 4.4. These values were found to give the best overall performance for motors up to the order of 1000W rating. Some adjustment can be made to the characteristics of the amplifier by the addition of external resistors, but unless it is for special applications it is recommended that the use of these should be avoided.

The AC gain is fixed by an internal feedback resistor and its value cannot be reduced. A resistor connected in series with capacitor C_3 between pins 1 and 4 can be used to increase the AC gain but this has the disadvantage that the soft-start function may not operate correctly, due to the fact that C_3 is pre-charged at switch-on as part of the soft-start sequence.

The DC gain is also fixed by the design of the amplifier but this can be reduced by means of an external resistor (R_1) connected in parallel with C_3, across pins 1 and 4. However, this suffers from two disadvantages. First the tolerance on the absolute value of feedback resistor can be as high as +75 and -50%. (Note that this does not affect the performance of the ZN411 normally since the design relies on the matching of internal resistors and not their absolute value.) This could mean that on a production line the value of the external feedback resistor may have to be separately adjusted for each unit incorporating the ZN411. Secondly the external resistor temperature coefficient will probably not match the internal resistors resulting in variations of regulation and dynamic response over the operating temperature range.

The frequency response of the amplifier can be adjusted by means of C_3 while the overall dynamic response of the system is also governed by the values of C_1 and C_2. The values of these capacitors are best chosen by experimentation with the ZN411 circuit connected to the actual motor/gear box/load combination to be used in the final product. The value of the soft start capacitor C_4 can also be verified at this stage. Only if satisfactory performance cannot be achieved by adjustment of these capacitor values should modifications of the AC/DC gain of the amplifier with external resistors be considered.

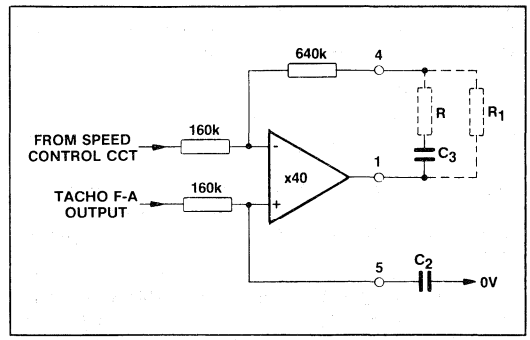


Fig.8 Schematic diagram of error amplifier

6. COMPARATOR RAMP GENERATOR

The comparator ramp circuit consists of a matched current source which is used to charge the timing ramp capacitor, C_6 connected to pin 12. A discharge transistor is connected from pin 12 to the 0V rail and this is switched on by the Voltage Sync logic for 200μs as the mains voltage passes through zero volts. Pin 12 is also connected internally to one input of the Comparator, the other input of which is connected to the Error Amplifier output. The ramp voltage therefore constitutes a timing reference signal which is reset at the start of each mains half cycle. The value of Ramp capacitor C_6 should be selected to produce a nominal 2.0V amplitude ramp at pin 12 with a charging current of 20 microamps.

Since $i = C\ dv/dt$

Then $C_6 = I_3/V_{ramp} \times 2f$

Where f = mains supply frequency

For V_{ramp} = 2.0V this gives:

$C_6 = 5/f$ (microfarads) ... (15)

The overall gain of the system is inversely proportional to the amplitude of the ramp signal. This fact can be used to provide some adjustment of gain by selecting different values of C_6 rather than using external feedback resistors as described in the previous section. The designer should take care to ensure that the negative peak amplitude of the ramp is always more positive than the minimum Error Amplifier output voltage, after taking into account all component tolerances. Failure of the ramp signal to meet this requirement will result in the speed control range being restricted at the low speed end of the conduction angle/motor speed characteristic.

7. VOLTAGE AND CURRENT SYNCHRONISATION

The function of the voltage synchronisation circuit is to produce a pulse symmetrical in time about the point when the mains voltage crosses zero volts. This pulse is then used to discharge the Ramp capacitor. If this pulse is not symmetrical then the ramp will start at a different time on alternate positive and negative half cycles producing a different triac firing angle for the two half cycles and resulting in a DC component being fed to the load, which in most cases is undesirable. Due to other circuit design considerations the input, pin 13, was referenced to the $-V_{CC}$ rail, whereas ideally the input threshold levels should be referenced to the 0V (neutral) rail in order to achieve symmetrical switching. In order to accomplish this the positive inut current threshold level was designed to be a factor of three times the negative current threshold. Hence by suitable choice of external resistor R_6, the voltage

threshold levels on the mains waveform can be calculated to produce values of +15V and -5V with respect to the -V_{CC} rail, which is ±10V with respect to the 0V rail.

The level is given by:

$$+V_{th} = I_{in} \times R_6$$

and

$$-V_{th} = -I_{in} \times R_6$$

where $\pm V_{th}$ are the threshold voltages with respect to -V_{CC} and $\pm I_{in}$ are the input currents given in the DC characteristics. A resistor of 330kΩ produces the correct levels.

The function of the Current synchronisation circuit is twofold, (a) to trigger the Output Monostable when driving inductive loads and (b) to generate a re-trigger pulse if for any reason the triac prematurely switches off before the end of the mains half cycle. The output Monostable is normally triggered by the Comparator when the ramp voltage crosses the Error Amplifier output level. However, when driving inductive loads at high conduction angles, the Comparator may have switched over before the load current from the previous half cycle has dropped to zero. In this case the trigger to the Output Mono is held off until the triac switches off as the load current drops below the triac hold current level. At this point the voltage acorss the triac will rapidly switch to the instantaneous value of the mains voltage, which depends on the phase lag of the load current. This voltage step is detected by the Current Sync input, pin 14 and providing that the Comparator output is already low, will trigger the Output Mono. The same thing occurs if the triac shuts off before the end of the mains half cycle causing the voltage across the triac to switch to the instantaneous level of the mains voltage. Unlike the voltage sync input it is not important that the current sync input be symmetrical about the 0V rail. The threshold current is nominally 110 microamps referenced to the -V_{CC} rail and so a 270kΩ input resistor (R_5) will produce a threshold voltage of typically ±30V.

Note that under certain conditions with a faulty triac that will not hold in the on state, the ZN411 will repetitively apply firing pulses to the triac. Due to the relatively high peak level of gate current compared to the ZN411 supply current this will, after several firing pulses, pull the device supply voltage below the Switch-on Reset level. In this situation a faulty triac can easily be mistakenly diagnosed as a malfunctioning IC.

8. TRIAC GATE OUTPUT

The triac Gate output circuit generates constant current negative going pulses, for more balanced firing of the triac, and allows direct connection between the ZN411 output and the gate terminal of the triac. The gate current level and pulse width are set internally in the ZN411 and are suitable for most types of small to medium power triacs (up to the order of 40A load currents). The maximum gate current can additionally be limited by means of an external resistor R_4. The only advantage in doing this would be, when using a sensitive gate triac, to allow the dropper resistor (R_7) wattage and capacitor value (C_8) to be reduced in value, since the normal gate current constitutes approximately 20% of the device supply current. See Section 3 for details of selections of components R_7 and C_8. The value of external limiting resistor can be calculated from:

$$R_4 = \frac{4.8 - V_{GT}}{I_G} - 6.5 \qquad \ldots (16)$$

where V_{GT} = Gate trigger voltage of triac
I_G = Gate current of triac.

9. CURRENT LIMIT

The current limit is set by the value of resistor R_3 connected in series with the load. The voltage dropped across this resistor by the load current is rectified and then integrated by capacitor C_7 in conjunction with a 160kΩ on chip resistor. The voltage on C_7 is used to switch the Limit Comparator which discharges the soft start capacitor, C_4, thereby reducing the triac conduction angle and hence load current until it falls below the trip level of the current limit circuit. This level corresponds to a mean voltage across R_3 of 540mV which is equivalent to 6A rms through a 100mΩ resistor (for a full sine wave). Some variations in the characteristics of the Current Limit circuit can be achieved by changing the value of C_7.

Generally the time constant of C_7 and the on-chip 160kΩ resistor should be of the order of several mains supply cycles (i.e. 100ms). A higher value will result in slower response of the circuit to an overload whereas a lower value will produce a fast response, but as the integrator time constant is reduced the circuit will react more to the peak rather than the average value of the current waveform. This will result in foldback of the torque/speed characteristic which may be a useful feature for some types of applications.

Note that the current limit facility should be used more as a torque limiting mechanism rather than as an overload protection for the motor. The problem with relying on the Current Limit circuit to protect the motor is that as the load is applied the motor characteristic will change from constant speed to essentially constant torque at the current limit point, see Fig.2. If the load is maintained then the motor speed will rapidly fall off towards zero. However, most small universal motors are cooled by a small centrifugal fan mounted on the armature which draws air through the motor casing past the windings. The cooling efficiency of this arrangement is very poor at low armature speeds causing most motors to rapidly overheat if the power is not removed within a short time under current limit conditions.

10. REVERSE SWITCH INPUT

This input was designed to operate in conjunction with a changeover switch which will reverse either field or armature connections of the motor. When a logic change of either polarity is detected at the REV input, pin 15, then the soft start capacitor, C_4 is discharged and held discharged until the motor speed falls to almost zero. At this time the hold on C_4 is removed, which enables the triac gate pulses and allows the motor to accelerate under control of the Soft Start Ramp. Without this function very high transient currents can flow in the armature, (leading to damage of the brushes and commutators) if connections are reversed with power applied and the motor in motion. Ideally a 3 pole break-before-make switch should be used with the switch pole for the Reverse input, timed so that it operates while the two poles used for the armature are open-circuit. This will ensure that the output drive will be removed before the armature connections are made when switching in either direction.

The Reverse input pin has an on-chip 40kΩ pull down resistor between the input and the -V_{CC} rail. This allows the use of a single way on/off switch to be used as the control pole of the changeover switch, so that with pin 15 open circuit the forward mode is selected. With pin 15 connected to the 0V rail the reverse mode is activated. Note that the speed is internally limited to 25% of the speed control range when in the reverse mode.

Note that if the motor reversing switch poles are omitted the Reverse control can be used to change the speed range of the motor. However, when the control switch is operated the motor speed will immediately be reduced to zero and will then run up to the new speed with a normal soft start.

SYMBOLS USED IN TEXT

Symbol	Definition	Relevant Section(s)
f	Mains frequency	6
f_T	Tacho frequency	4
I_1	Current source value, pin 10	4
I_2	Current source value, pin 9	4
I_{CC}	Chip supply current	2
I_{ext}	External circuitry DC supply current	2
I_G	Triac gate output current, pin 3	2,8
I_S	Total DC supply current	2
N	Armature speed	4
P	Number of tacho poles	4
P_d	Power dissipation	2
t_G	Triac gate pulse width	2
t_{mono}	Tacho monostable time period	4
t_{ss}	Soft start time period	3
V_1	DC voltage on C_9	2
V_{AC}	Mains AC supply voltage (rms)	2
V_{CC}	DC voltage on pin 2	2
V_{DC}	Unstabilised DC supply voltage	2
V_G	Triac gate output voltage, pin 3	8
V_{GT}	Gate trigger voltage of triac	8
V_r	Ripple voltage on C_9 (p-p)	2
V_s	Shunt regulator voltage	2
V_{wkg}	Maximum working voltage of C_9	2
V_{ramp}	Ramp amplitude, pin 12 (p-p)	6
V_{ref}	Control reference voltage, pin 8	4
$\pm V_{th}$	Voltage sense threshold voltages	7
$\pm V_{TH}$	REV input threshold voltage	10

Table 2

System Design with the ZN1060E

The ZN1060E includes (refer to Fig.1):

1. Oscillator
2. Error amplifier
3. Pulse width modulator
4. Voltage reference
5. Control logic
6. Stop-start circuit
7. Loop fault protection
8. Duty cycle limit and low supply operation
9. Secondary current monitoring

Whereas items 1 to 5 will be found on any switching converter IC the ZN1060E provides the additional features of items 6 to 9, these are described in the following notes.

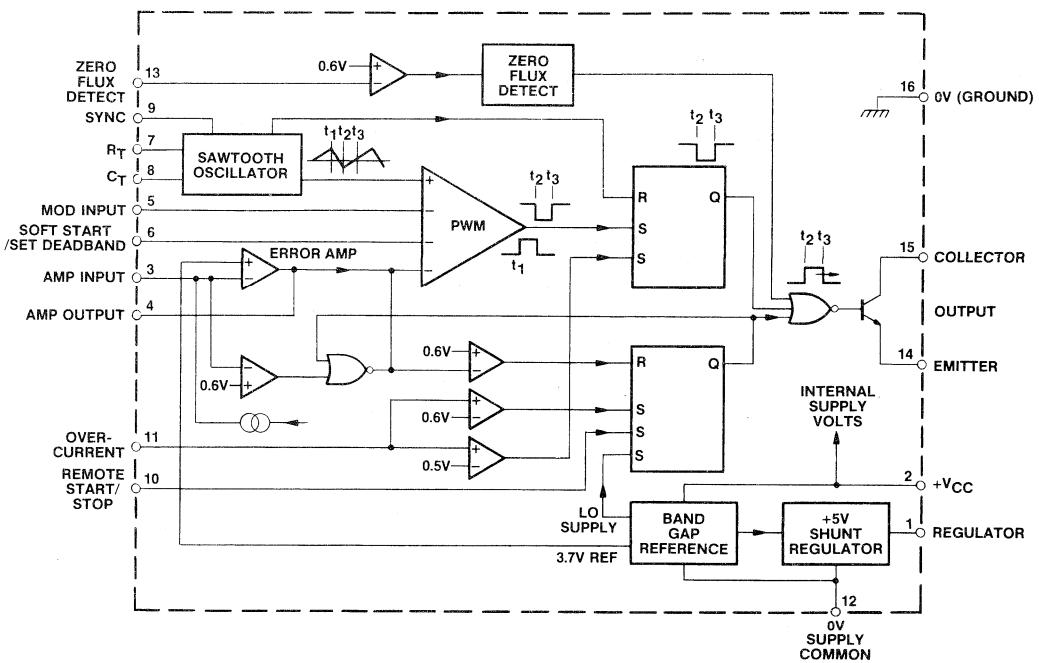


Fig.1 Block diagram

STOP-START CIRCUIT (Refer to Figs.2, 3 and 4)

The RS bistable can be set by three different functions:

1. Remote on/off control on pin 10.
2. Current monitoring on pin 11.
3. Low voltage protection (internal monitoring).

As soon as one of these functions cause a setting of the bistable, the output pulses are blocked via the output gate. At the same time transistor TR1 is switched-on resulting in a discharge of the soft start capacitor on pin 6. The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead time, the output starts with a very small gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This automatic reset mode limits the energy during fault conditions. The realisation and the working of the circuit is indicated in Fig.2. The dead-time and soft start are determined by an external capacitor that is connected to pin 6, the duty cycle programme pin (Δmax. setting).

The discharging current is limited by an internal 50Ω resistor in the collector of TR1. The voltage at pin 6 descreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the bistable is reset. The output stage is no longer blocked and TR1 is cut off. Now V_Z will charge the capacitor via R1 to the normal maximum voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on pin 3, or by the static Δmax. setting on pin 6 (see Fig.4).

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logic signal. This can be done via the TTL-compatible remote on/off input on pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage of 2V or more is applied. Starting up occurs via the slow-start circuit.

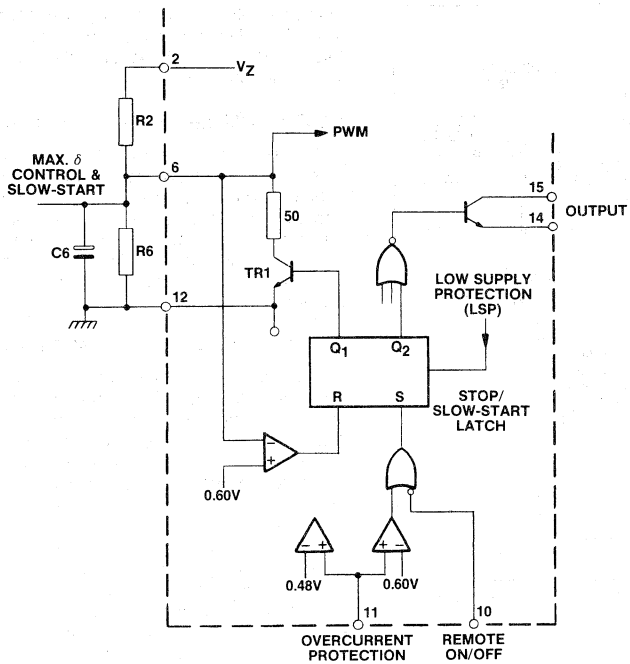


Fig.2 Stop/slow-start circuit

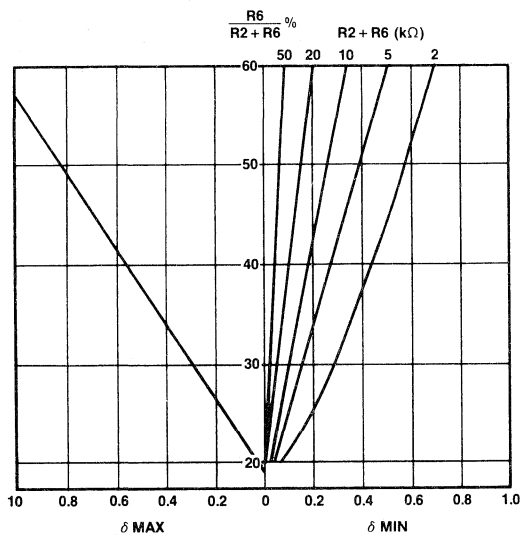


Fig.3 Typical end stop characteristic

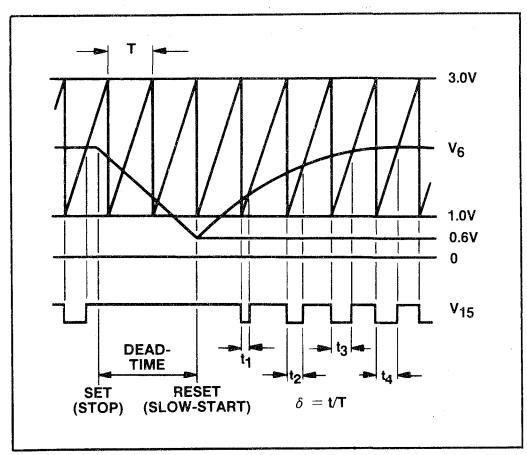


Fig.4 Waveforms associated with the stop/slow-start circuit

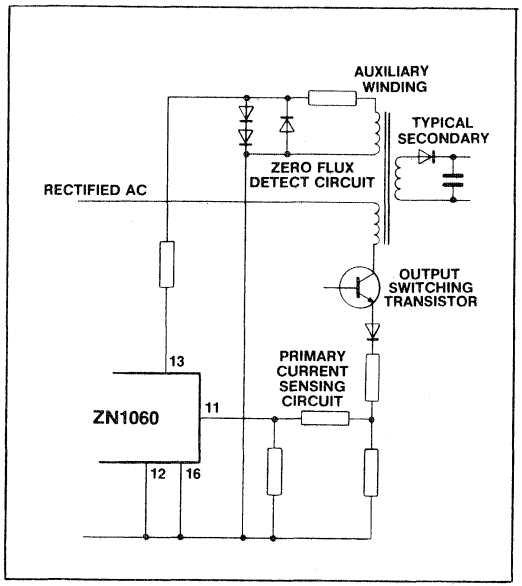


Fig.5 Current monitoring (see Fig.11 for component values in a 240V AC application)

LOOP FAULT PROTECTION

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via the resistor connected between pin 3 and pin 4 (3-4). This would result in a large duty cycle. A current source on pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3-4). As a result, the duty cycle will become zero, provided that R(3-4) > 100k. If the feedback loop is short circuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore an additional comparator is active for feedback voltages at pin 3 below 0.6V and an internal resistor of typically 1k is shunted to the impedance on the Δmax. setting pin 6. Depending on this impedance, Δ will be reduced to a value of Δ_0, typically 1% of the total period.

DUTY CYCLE LIMIT AND LOW SUPPLY OPERATION

A potential divider across V_Z and connected to pin 6 allows external adjustment of the duty cycle Δ from 0 to 95%. In the flyback system Δmax. = 45% and Δ_0 = 1% i.e. approximately 2μs. Further Δ is maintained at zero as long as the chip supply remains below V_Z. A capacitor connected to pin 6 can be used to slow down the rate of increase of Δ from zero to its normal value. A soft start characteristic is thus obtained (see Fig.4).

SECONDARY CURRENT MONITORING (PIN 13)

The function of this circuit is to provide complete protection against all secondary overload effects with automatic reset. It is only after this input signal has disappeared can a new period of primary current start.

This information can be taken from an auxiliary winding on the output transformer tht gives a signal similar to the primary collector voltage but referenced to zero voltage as shown in Fig.5.

As long as the secondary current has not decreased to zero, the primary collector voltage remains high. At the time the secondary current becomes zero the collector voltage on the output transistor decreases to V_{CC} (rectified mains) and stays at this level until the beginning of the new primary current low. On the auxiliary winding the voltage remains positive during the flow of secondary current; it stays at zero during the time there is no primary or secondary current and is negative whilst primary current flows.

In the ZN1060E a comparator detects this positive voltage. It has a 600mV sensitivity to take account of the secondary short circuit case. If there is a secondary short circuit, the secondary winding is only loaded by a single diode carrying a high current. The voltage across the secondary winding will then be only about 1V. To minimise power losses and utilise a convenient winding ratio a comparator of this sensitivity is required. The logic processor ignores ringing on the input waveforms.

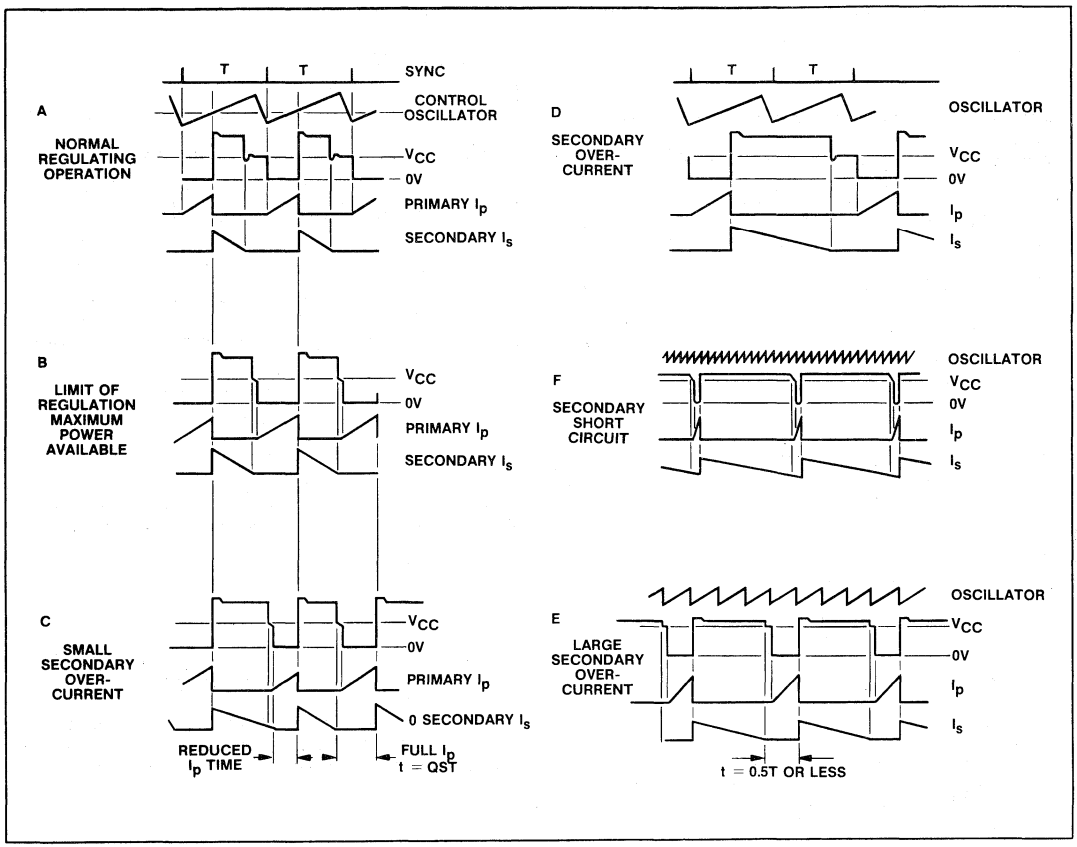


Fig.6 Complete energy transfer flyback operating waveforms

OPERATING PRINCIPLE

The operating principle chosen is a Complete Energy Transfer (CET) system in which the primary current can only flow if the secondary current has reached zero, i.e. there is zero flux in the transformer core. The various possibilities are shown in the waveform diagrams in Fig.6 which should be consulted.

Fig.6A - Normal Operation. The primary current flows in an essentially linear mode from 0 to I_{max} and then decreases very rapidly to zero. The secondary current then flows and decreases in a linear mode to zero. In normal regulating operation there is a dead period after the secondary current has stopped. During the dead time, the primary voltage reduces from about twice Vcc to Vcc. The ringing is due to leakage inductance and stray capacitance.

Fig.6B - Maximum Power. When the secondary power increases the control loop makes the primary flow sooner and the secondary circuit flows for a longer time. In the limit case when maximum output power is demanded, the primary current starts just after the previous secondary current has reached zero. This is the limit of regulation and the power is fixed by Vcc and the primary inductance.

Fig.6C - Small Overload. If the overload current continues to increase, the secondary current can continue to flow for longer than the total period. The following primary current pulse is inhibited but the next primary current pulse flows for a full half period.

Fig.6E - Large Overload. If there is an even greater secondary overload the primary current will be inhibited during several periods.

Fig.6F - Secondary Short Circuit. If the secondary is short circuited a large number of primary current pulses are inhibited until complete energy transfer has been completed and the secondary current has reached zero. Then a new normal primary current pulse will occur over a full half period.

It can thus be seen that with this principle complete protection is provided against secondary overcurrents or short circuits with automatic reset. It also provides a starting mode, because at switch-on, the secondary filter capacitors are effectively a short circuit, until they are charged up.

The pulse width modulation characteristic for the ZN1060 is shown in Fig.7. Refer to Fig.4 for the voltage waveforms and timing references.

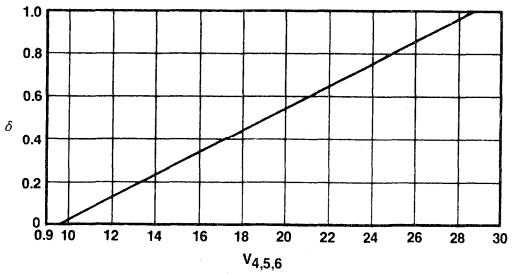


Fig.7 Typical PWM characteristic

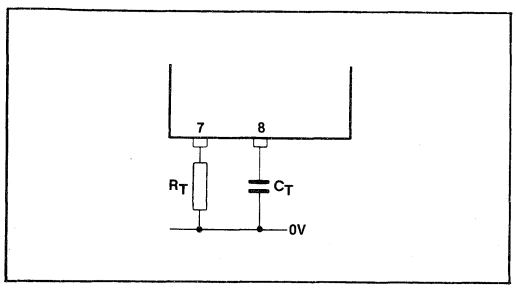


Fig.8 Oscillator frequency. The oscillator frequency is determined by R_T and C_T. The values of C_T and R_T are obtained from Fig.9 to give the required operating frequency of the ZN1060.

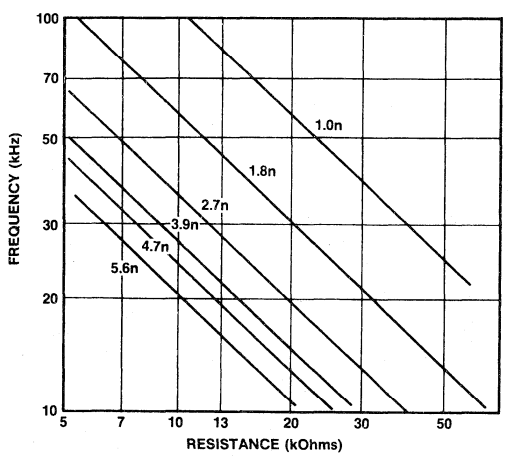


Fig.9 Typical oscillator operating frequency

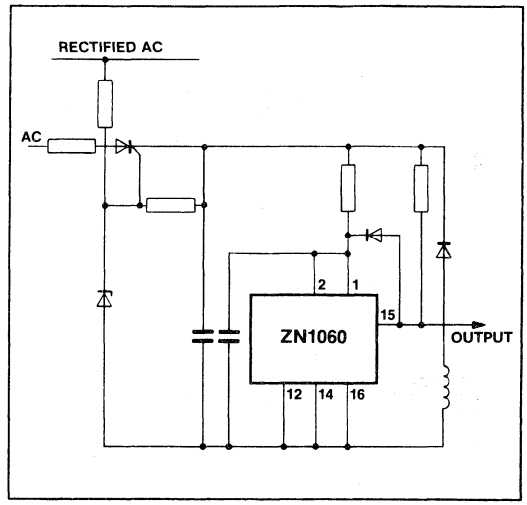


Fig.10 Powering the ZN1060 (see Fig.11 for component values for use in a 240V AC application)

APPLICATION

Fig.11 shows the schematic diagram for a 150W 'off line' multiple output CET flyback circuit designed specifically for use in advanced European colour TV receivers. The design fulfils all the relevant specifications (V.D.E., CENELEC, B.S. etc) with regard to noise EMI and safety. The operating frequency of the ZN1060 is 25kHz as shown by Fig.9.

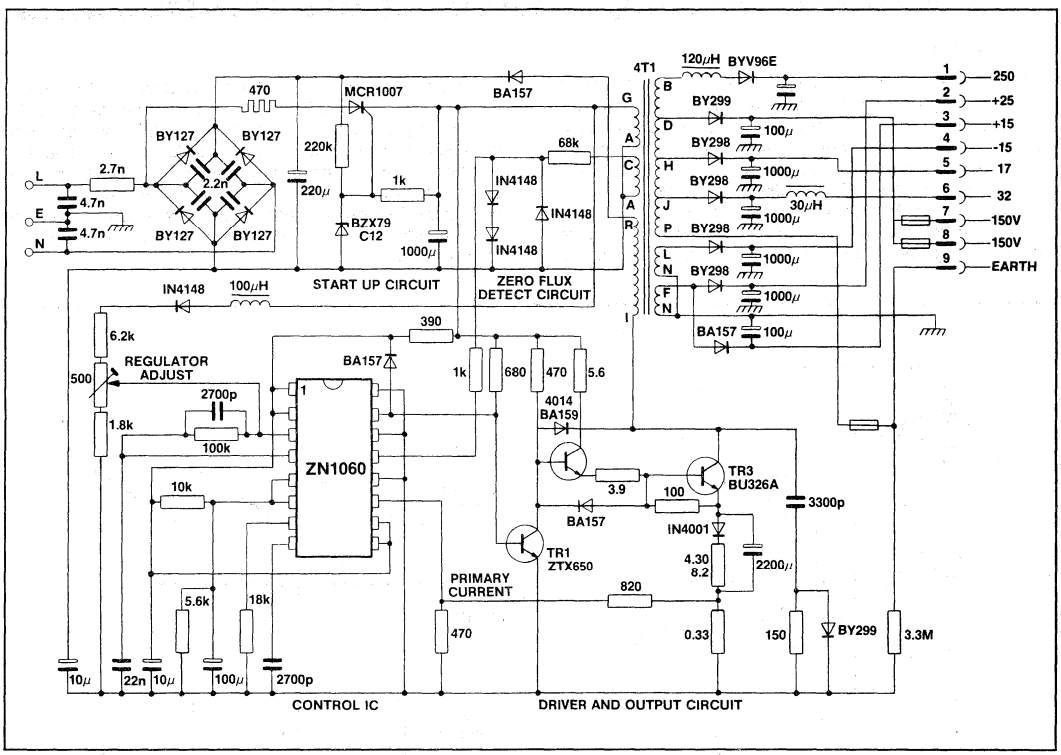


Fig.11 Power supply schematic

OSCILLATOR

The oscillator can be programmed, by means of an external timing resistor R_T and capacitor T_T, to define any time period in the range 2 seconds to 2 microseconds, (0.5Hz to 500kHz). The oscillator period is approximately $t_{OSC} = 0.28\ C_T R_T$ where t_{OSC} is in microseconds when R_T is in ohms and C_T in microfarads. $3k \leqslant R_T \leqslant 100k$; $C_T \geqslant 1500pF$.

Fig.1 illustrates the operation of the oscillator.

The discharge time of C_2, t_N, determines the width of the oscillator output pulse and the ramp reset time. In order to achieve satisfactory reset of the ramp generator the value of C_T must be at least 2.7 times that of the ramp capacitor C_R. For most practical applications $C_T = 3C_R$ will be found satisfactory. The oscillator pulse width is also used as a blanking pulse to both outputs to ensure that there is no possibility of having both outputs on simultaneously during transitions. The output dead time can be estimated from the relationship: $t_N = 95\ C_T$ microseconds when C_T = microfarads.

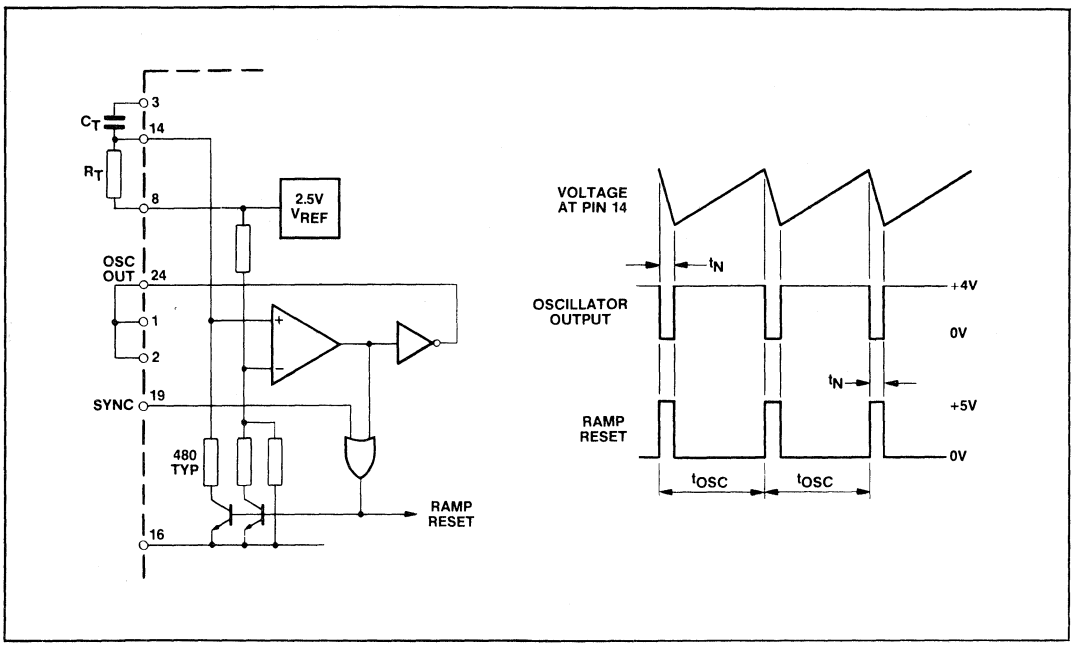


Fig.1 Oscillator equivalent circuit

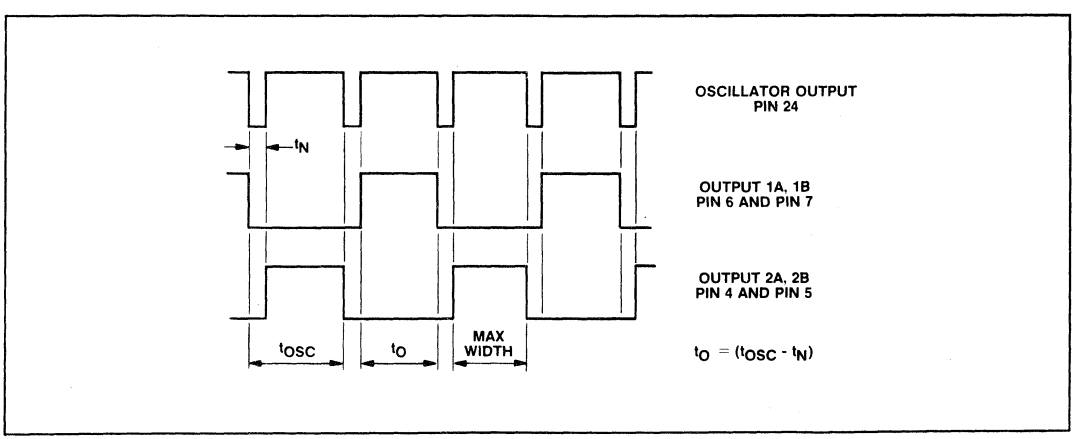


Fig.2 Relationship between oscillator and output waveforms

The frequency of the output waveform is approximately $f_o = 1.8/C_T R_T$. Note that f_o refers to the frequency of the outputs 1A, 1B (pins 6 and 7) or outputs 2A, 2B (pins 4 and 5). The frequency of the oscillator and ramp generator waveforms is twice f_o.

The oscillator period, t_{OSC}, is virtually independent of the supply voltage down to V_{CC} = 2.6V. Further, the timing period will generally change by less than ±0.5% for a ±50°C change in ambient temperature and the variation in timing period from one device to another is normally less than ±2% assuming R_T and C_T are kept constant.

If it is desired to synchronise a ZN1066 to an external clock, a pulse of +1V to +5V may be applied to the SYNC input pin 19, with $C_T R_T$ set slightly greater than the clock period. The width of this clock pulse should be greater than 0.2μs. If pin 19 is not used it can be left open cicuit or connected to low current ground.

RAMP GENERATOR

The simplified equivalent circuit of the ramp generator is shown in Fig.3.

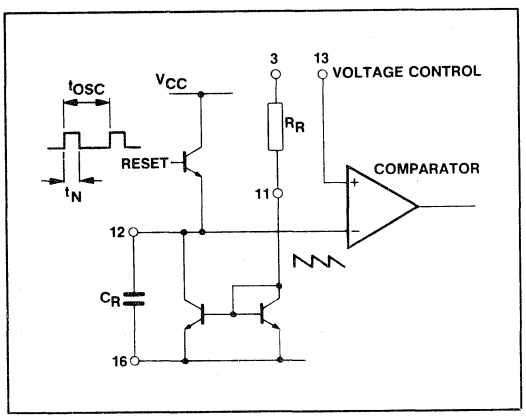


Fig.3 Ramp generator and pulse width modulator

The ramp generator is driven by the reset pulse from the oscillator to charge the ramp timing capacitor C_R to 4.3V. This charge time must be sufficiently long to ensure that the ramp generator is reset to at least 4V. This condition is met by making $C_R \leq 0.33\ C_T$. At the end of the reset pulse C_R is discharged by a constant current defined by the ramp timing resistor R_R. The period of the ramp generator is identical to the oscillator timing period T_{OSC}. The amplitude of the ramp is approximately $V_R = 1.33\ C_T R_T/C_R R_R$ which for a ramp amplitude of 3V pk-pk and $C_R = 0.33\ C_T$ gives $R_R = 1.3R_T$. $4.3k \leq R_R \leq 100k$; $C_R \geq 330pF$.

Fig.4 shows the operating conditions for the ramp generator and pulse width modulator circuits.

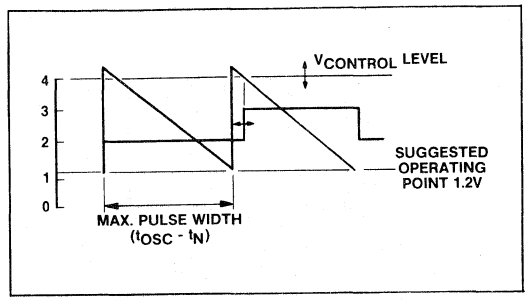


Fig.4 Pulse width modulation

The ramp will cross the comparator reference point ($V_{control}$ level) at essentially the same time after set up independently of supply voltage and temperature. Due to the matching of on-chip components ramp linearity is maintained to within 2%; there is relatively little variation in performance from integrated circuit to integrated circuit when using a given set of external components. This is beneficial in avoiding the need for individual adjustment once a design has been finalised.

THE VOLTAGE REFERENCE

The temperature coefficient of V_{REF} is typically ±50ppm/°C max.). The output current capability is 1mA. If increased current capability is required a resistor may be connected between pins 3 and 8. The maximum sink current of V_{REF} is 10mA which limits R_2 to a minimum value of 270Ω; the temperature coefficient is independent of the current. See Fig.5.

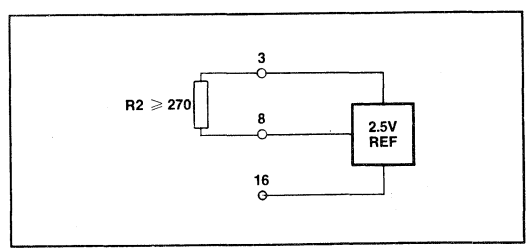


Fig.5 Extending the current capability of V_{REF}

CONTROL AMPLIFIER

These circuits are general purpose, wideband, differential input voltage amplifiers. The frequency response curves of Fig.6 show the uncompensated amplifier with poles at approximately 240kHz, 7MHz, 20MHz and a unit gain crossover at 45MHz. The amplifier is compensated by connecting a 0.02μF capacitor from the output to pin 16, the single earth point. The compensated curve has a single pole at approximately 10kHz and a unity gain crossover at 10MHz.

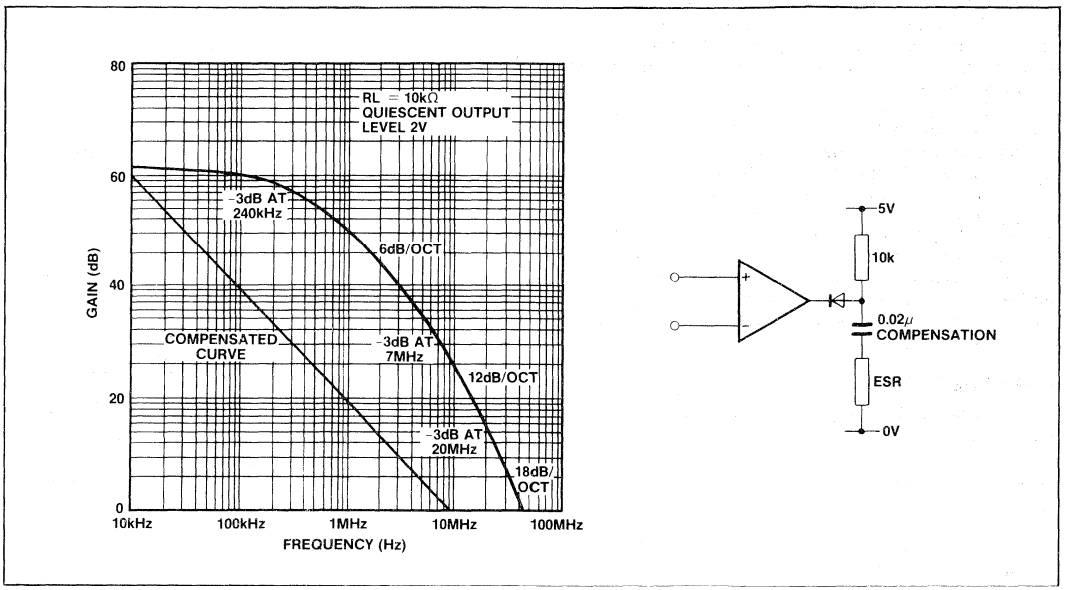


Fig.6 Amplifier open loop gain as a function of frequency

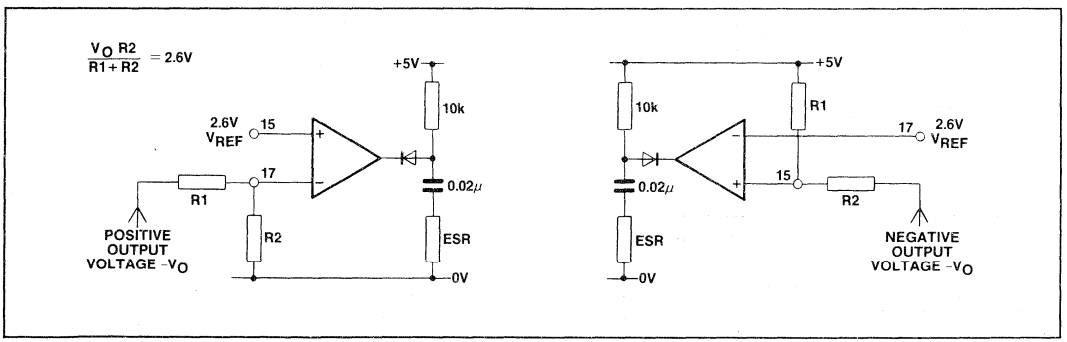


Fig.7 Voltage control biasing networks

With compensation, both amplifiers are stable in either the inverting or non-inverting mode. Fig.7 shows typical biasing circuits for achieving voltage control of positive and negative output voltages. Regardless of the connections, however, input common mode limits must be observed or output signal inversion may result.

LOOP STABILISATION

Most output filter designs will introduce one or more poles at a relatively low frequency. Typically 300Hz to 2kHz. One approach to the loop stability problem is to connect a series RC network which introduces a zero to cancel one of the output filter poles. In practice it has been found that better overall system performance is achieved using the technique outlined in Fig.8

A good starting point is to select the time constant of $R_F C_F$ to be approximately equal to the series resonant frequency of the output filter.

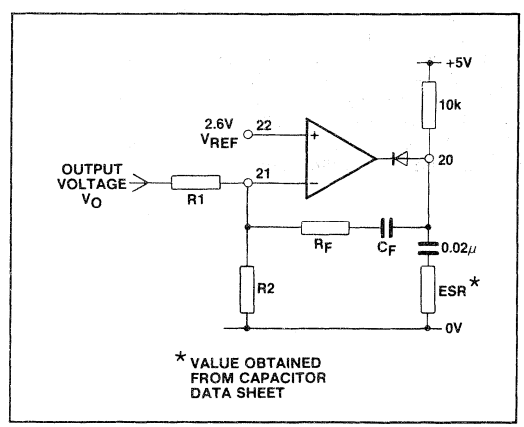


Fig.8 Closed loop stabilisation

CURRENT LIMITING

The output current is controlled indirectly by regulating the voltage drop Vs across a series sensing resistor Rs, the voltage to be regulated being the potential drop caused by the load current flowing through Rs. Whatever Vs drop is chosen its magnitude represents the total amount of load current. To minimise power dissipation in Rs, the size of the sampling drop Vs should be made as small as possible. However the problem of regulating a very small voltage drop should be taken into account and for most practical designs Vs = 0.05V is a good choice. The maximum power dissipated in Rs is then only 1% of the output power.

To obtain a near perfect constant current characteristic, as distinct from simple current limiting, it is necessary to feedback a small signal proportional to the output voltage of the regulator. Fig.9 shows the circuit developed for an off line switched mode power supply designed to deliver 0 to 20 amps at 5V DC.

The foldback current limiting characteristic shown in Fig.10 is obtained by increasing the value of R in Fig.9 i.e. the amount of feedback proportional to output voltage. In this way the short circuit current can be reduced to essentially zero.

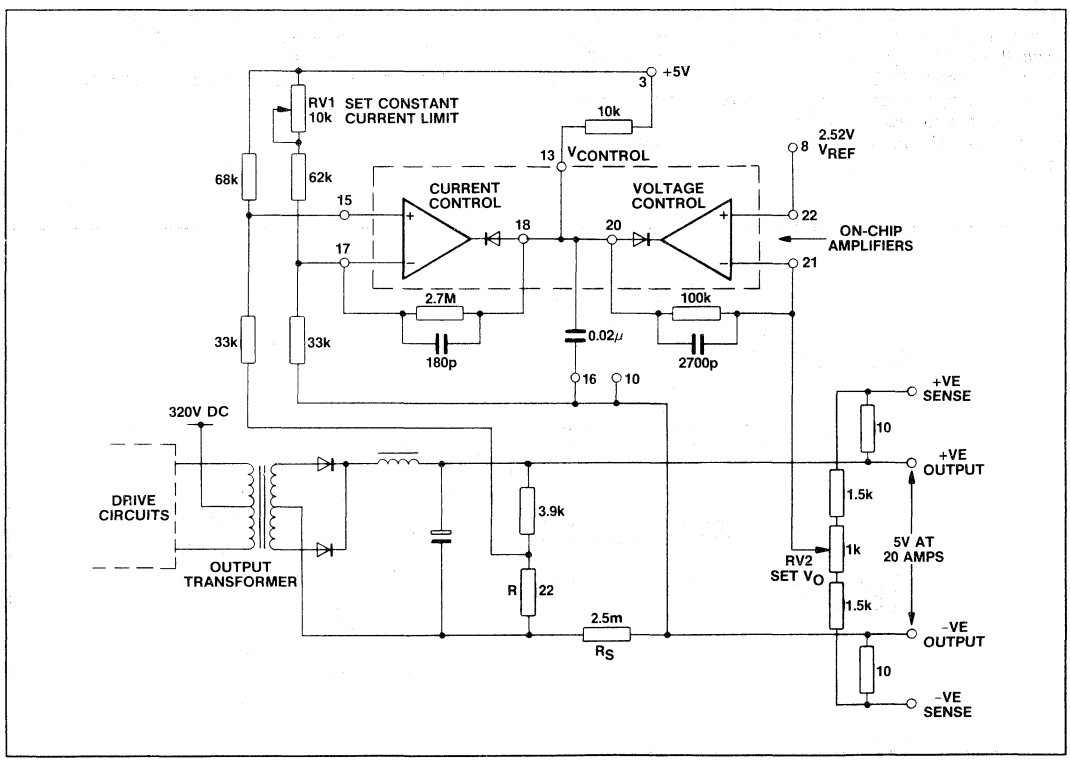


Fig.9 Current and voltage control circuit

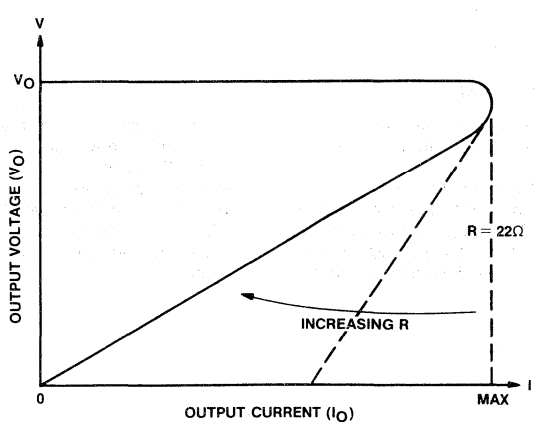


Fig.10 Output current cut-off

AUTOMATIC CROSSOVER

An automatic crossover power supply is unique in that it cannot be overloaded; it operates with full control into any load resistance from infinity to zero ohms. From infinity to the crossover resistance $= V_o/I_o$ max. it behaves as a voltage regulator holding its output constant as the current increases. From the crossover resistance down to zero ohms the power supply behaves as a current regulator, the terminal current being held constant as the output voltage decreases.

Since the voltage and current controls are each independently adjustable throughout the full voltage and current output range, the crossover point, which is the intersection of the two control settings, can be located anywhere in the volt-ampere range of the power supply. The curve in Fig.11 illustrates this type of operation and Fig.9 shows the circuit details, I_o max. being set by varying RV1 and V_o, by varying RV2.

The amplifier may also be used to sense primary current and produce a constant current characteristic or shorten an output pulse should transformer saturation occur. See Fig.12.

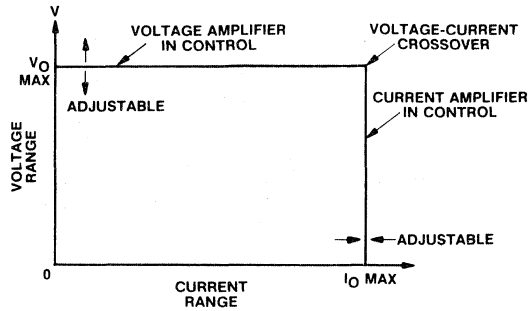


Fig.11 Automatic crossover, V/I characteristic

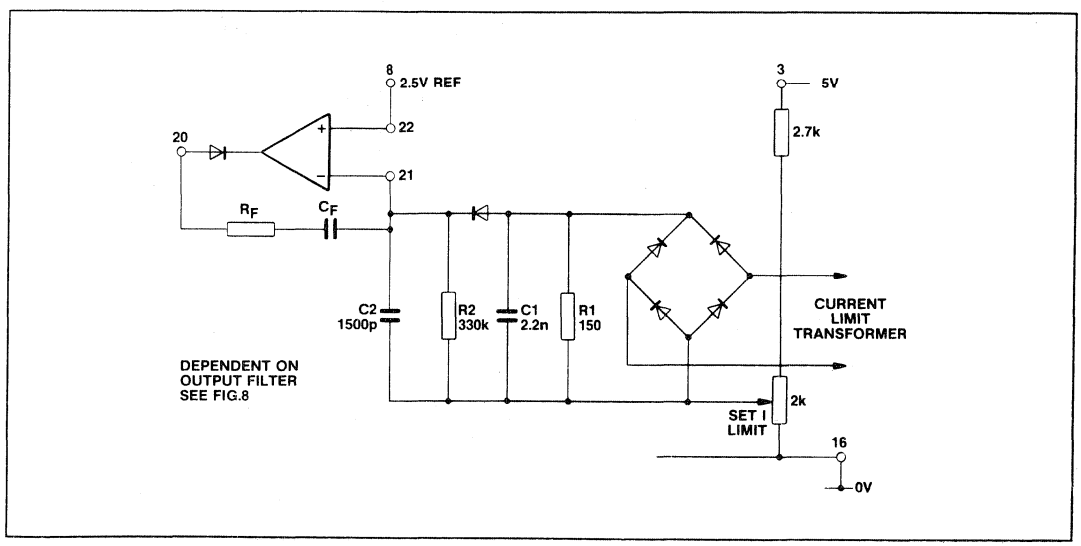


Fig.12 Constant current limit - sensing primary current

CYCLE-BY-CYCLE CURRENT LIMIT

If the design calls for protection against overcurrent in the external switching transistors then the circuit shown in Fig.13 may be used.

When the peak collector current in either output transistor exceeds a preset level, (set by RV1), the monostable comprising TR1 and TR2 trips. Activating the trip causes a direct cut-off to be applied to the gates which control the output stage and rapidly removes the drive to each of the output transistors and at the same time these reset the soft start circuit. Many power switching transistors have wafer thermal time constants in the 5ms region, and a monostable delay time of at least 50ms is recommended to allow the wafer to cool after an overstress.

This protection mechanism protects the power switching transistors even from the effects of a saturating power transformer.

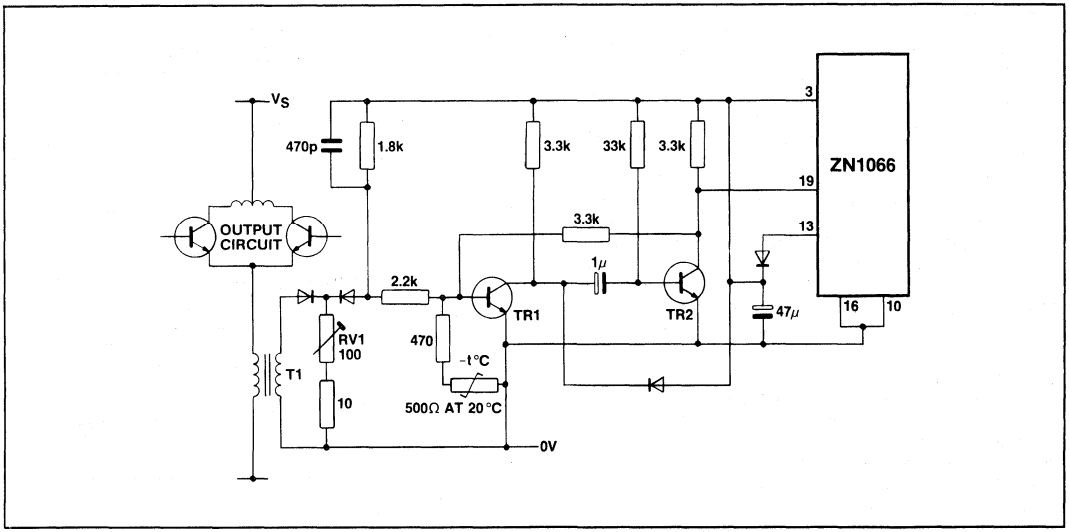


Fig.13 Current limit - primary side

OPTO-ISOLATION

When the ZN1066 is used to directly drive the output switching elements it is possible using the circuit outlined in Fig.14 to provide wideband input/output isolation. The two on-chip amplifiers combine with two opto-isolators to produce a tracking voltage source.

Temperature effects are largely confined to the opto-isolators. If these have matched characteristics and are isothermally mounted, the circuit has for most applications an acceptably low temperature coefficient. A dual opti-isolator package is a possible alternative.

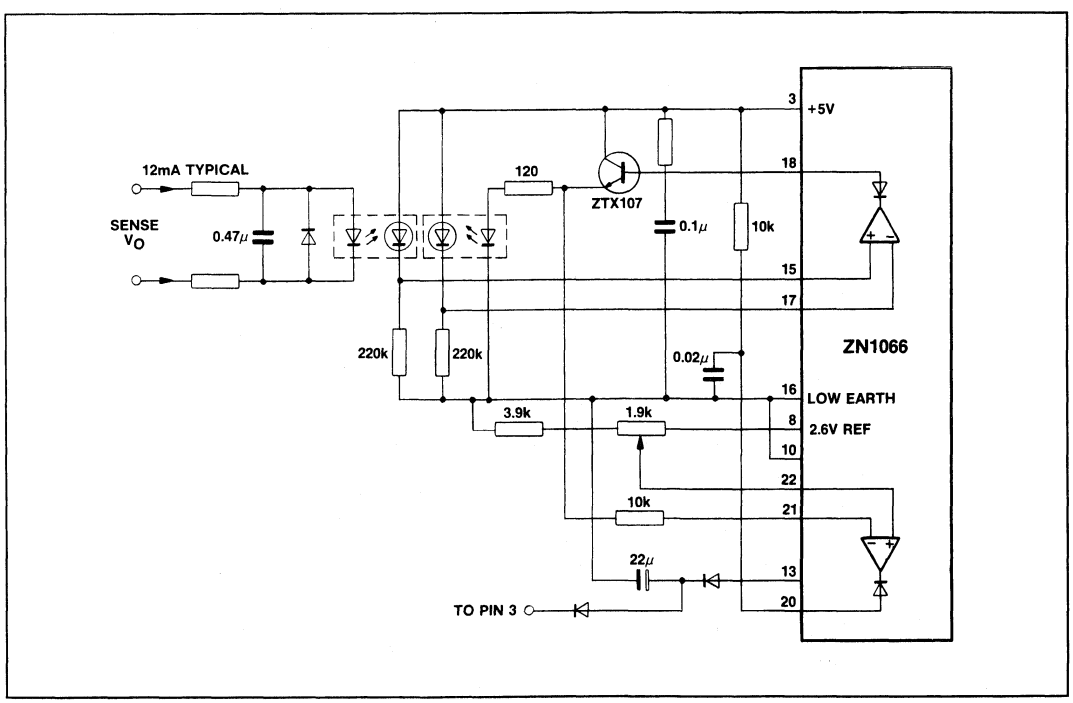


Fig.14 Opto-isolator control circuit

SOFT START

In most switched mode power supplies a soft start feature is required to prevent output voltage overshoots and magnetising current imbalances in the power transformer primary. This feature forces the duty cycle of the switching transistors to increase gradually from zero to their normal operating point during a system power up or after an inhibit. This function is easily implemented with the ZN1066 and one method is shown in Fig.15.

After an inhibit command or during power up, the voltage at pin 13 rises exponentially from zero volts toward V_{CC} with a time constant of R1 and C1, thus permitting a gradual increase in duty cycle. Diode D1 provides an OR function at $V_{control}$ pin 13, while TR1 serves to reset the soft start timing capacitor, C1, when an inhibit command is received thereby resetting the soft start function. D2 allows C1 to reset when the power is turned off.

CROSS COUPLED INHIBITS

One method adopted to try and prevent simultaneous conduction in the output switching transistors is to limit the maximum pulse width of the drive circuits so that a known off state time is defined. (Dead time. See Fig.16).

Unfortunately the storage time varies between any two power switching devices and the variation in storage time with temperature, loading and time is unpredictable. With modern switching devices a spread of 0.3 to 10μs is not uncommon. To be 100% safe the dead time should be in excess of 10μs and when one considers that at an output frequency of 20kHz the 100% pulse width is only 25μs it is not difficult to see that dead time setting severely limits the range of control. The output transformer must therefore have a higher turns ratio to give full output at minimum input voltages, leading to shorter higher current input pulses and loss of efficiency.

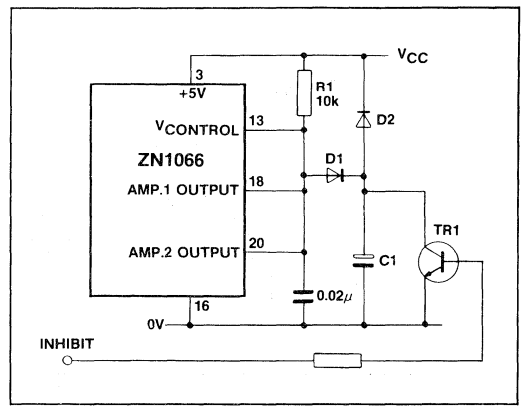


Fig.15 Soft start and inhibit

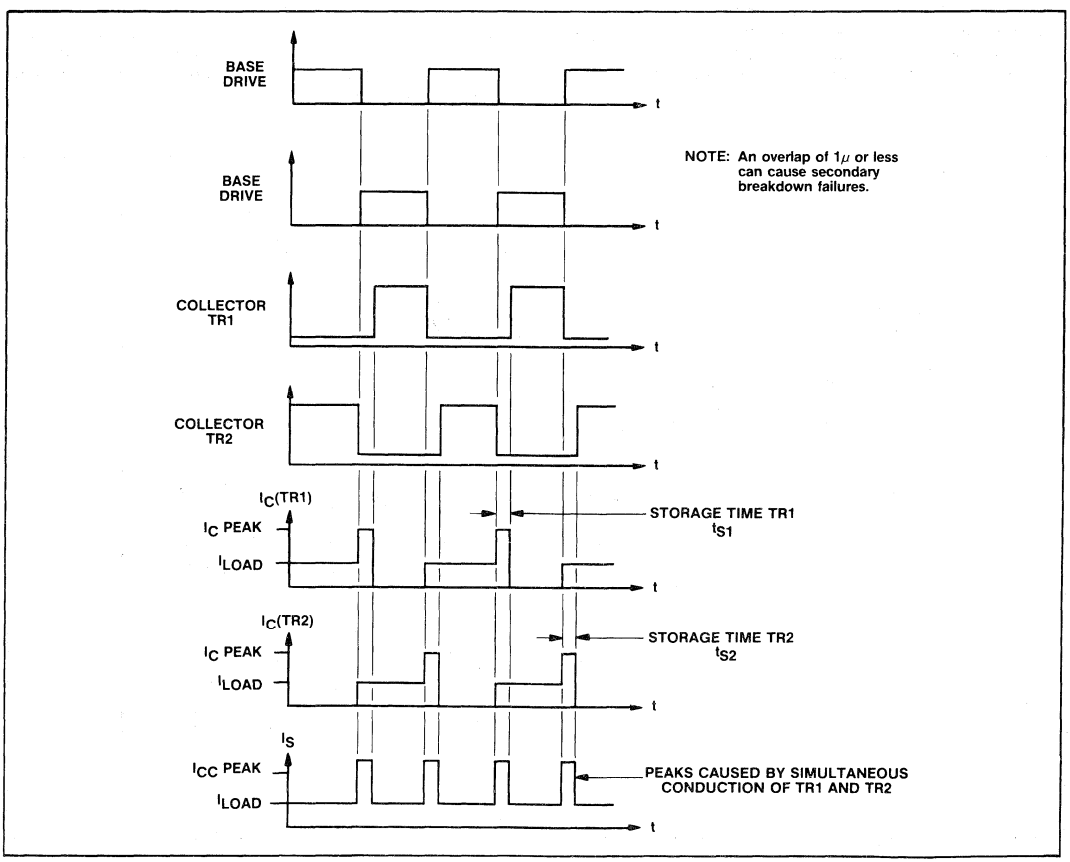


Fig.16 Effects of cross current conduction (overlap)

A foolproof solution to this problem is possible using the cross coupled inhibit feature of the ZN1066. The action of this circuit is shown in Fig.17.

Two fast acting inhibits, pins 1 and 2 are connected to the inputs of the pulse steering gates. A logic '0' at these inputs corresponds with zero drive output. These inhibit pins are effectively cross coupled to the power switching transistor collectors, either directly or via a separate winding specifically wound for this purpose. The storage time delay is sensed and feedback prevents one transistor from turning on until the other is turned off.

If a 100% pulse width drive is now applied to the bases of TR1 and TR2, cross current conduction is prevented since one transistor base drive is inhibited until the collector voltage of the other transistor has risen to the supply voltage, i.e. the transistor has turned off, irrespective of storage time. The cross coupled inhibit feature therefore automatically compensates for variations in storage time and allows up to 100% output pulse widths without overlap.

When both output transistors are in the OFF state, i.e. pulse widths less than maximum, then the logic '1' required for normal operation is conveniently obtained by connecting a suitable value resistor from each inhibit pin to pin 24. See Figs. 17, 33 and 34. Alternatively the centre tap on the feedback winding can be connected to pin 3.

Dead time settings (end stop) is therefore no longer required and the conflict between safe minimum off time and maximum control range no longer exists.

INRUSH CURRENT LIMITING

Since many switched mode power supplies are operated directly off the rectified 240V AC line with capacitor input filters, some means of preventing rectifier failure due to inrush current is usually necessary. One method which can be used is shown in Fig.18.

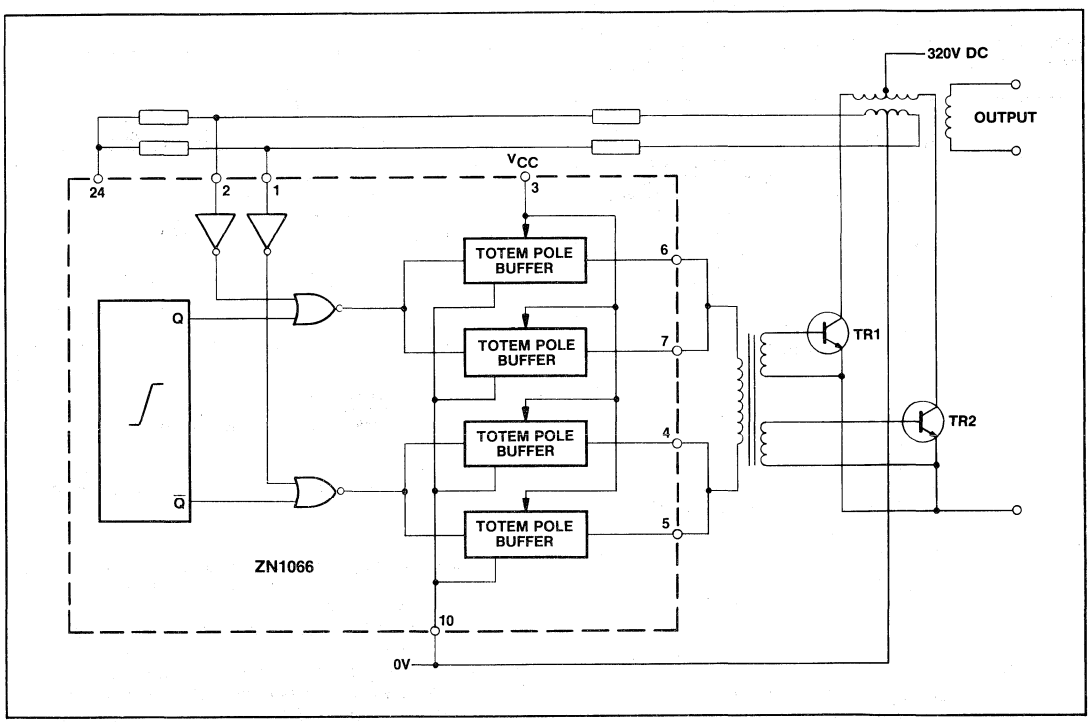


Fig.17 Automatic overlap control

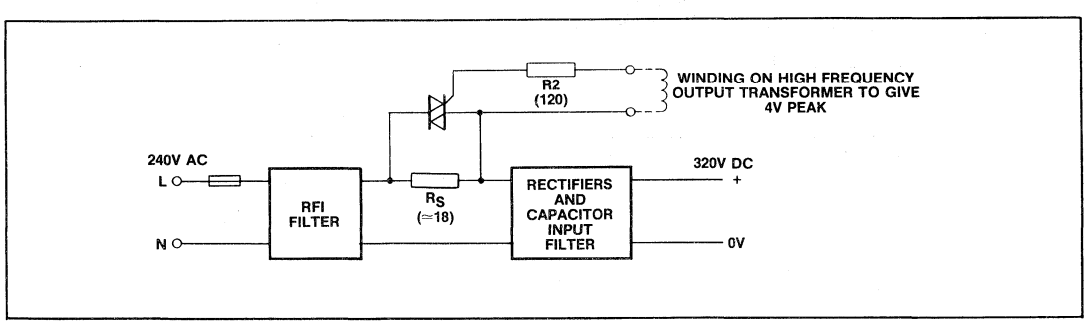


Fig.18 Inrush current limiting

In this circuit a series resistor Rs, is used to provide inrush surge current limiting. After the input filter capacitor has charged and converter action starts, a separate winding on the high frequency transformer applies drive to the gate of the input triac via R2 so that Rs is bypassed and its dissipation reduced to near zero.

A major advantage of this system is that the triac is brought into conduction at a time when the input capacitor is nearly fully charged so that the surge current is low.

OTHER CIRCUITS

The ZN1066 provides four identical push pull totem pole type outputs each capable of sinking and sourcing 60mA. The equivalent output circuit is shown in Fig.19.

Outputs may be paralleled for greater output drive. The totem pole type output is the most flexible and versatile possible.

In considering the application of the ZN1066 to switching regulator circuitry, there are a multitude of output configurations possible. The following diagrams do not exhaust the possibilities but serve mainly to illustrate some of the more common types of connections. See Figs. 20 to 27.

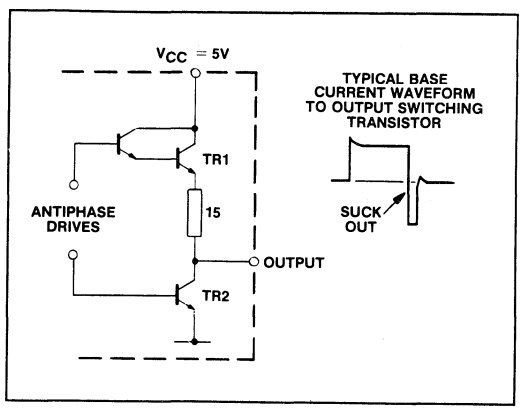


Fig.19 Output drive circuit (1A, 1B, 2A and 2B)

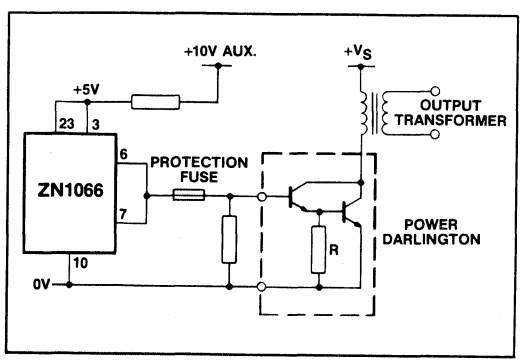


Fig.20 Direct drive for single ended or flyback converters

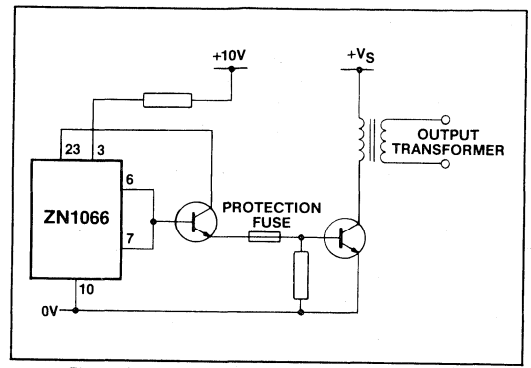


Fig.21 Alternative direct drive for single ended or flyback converters

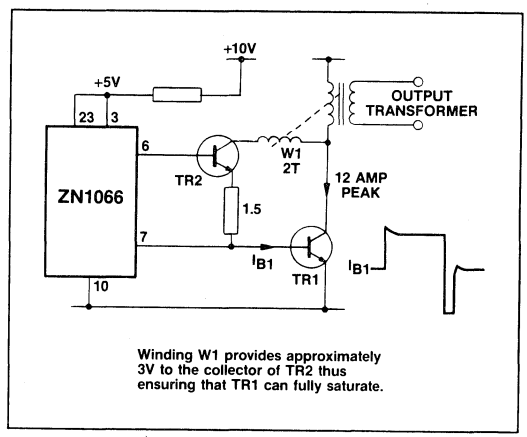


Fig.22 Direct drive for high power single ended converters

The main advantage of the connection shown in Fig.22 is that the current suck-out capability is maintained and TR1 can be rapidly turned off.

The windings W1 and W2 (see Fig.24) are connected in antiphase to the main primary winding. These windings provide an auxiliary supply of about 2.5V for the transistor TR3 and TR4 thus ensuring saturation of the Darlington pair. Peak collector currents in TR1 and TR2 excess of 12 amps are possible using this method of drive.

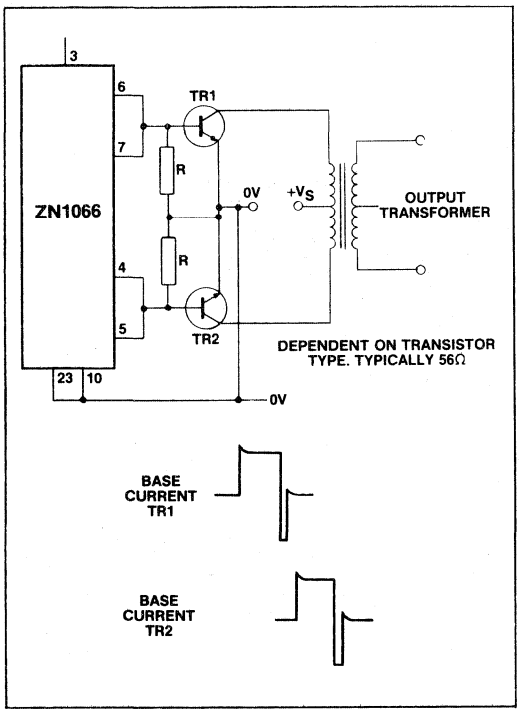


Fig.23 Typical direct coupled push-pull circuit

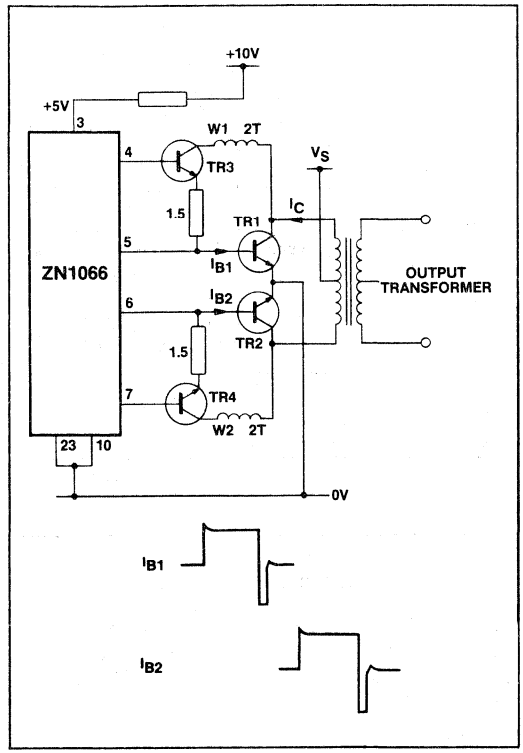


Fig.24 High power direct coupled push-pull circuit

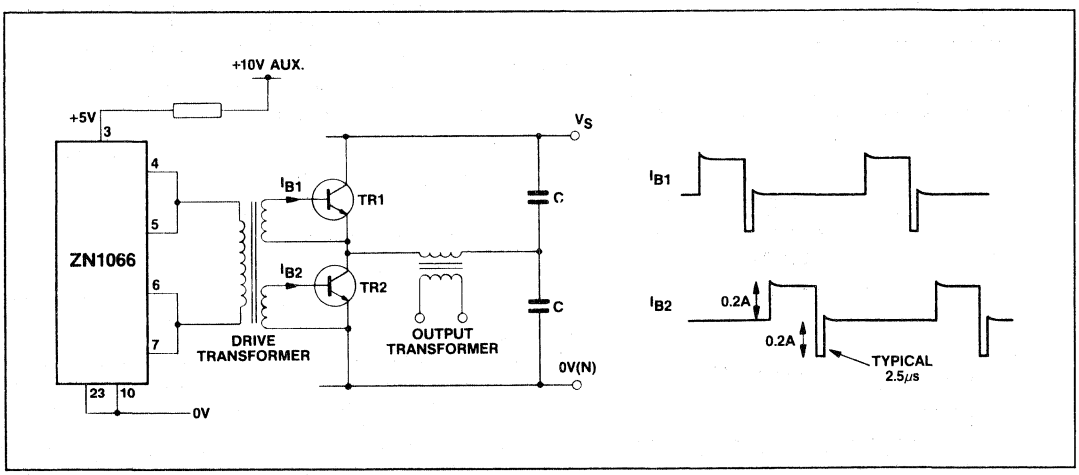


Fig.25 Transformer coupled half bridge push-pull circuit

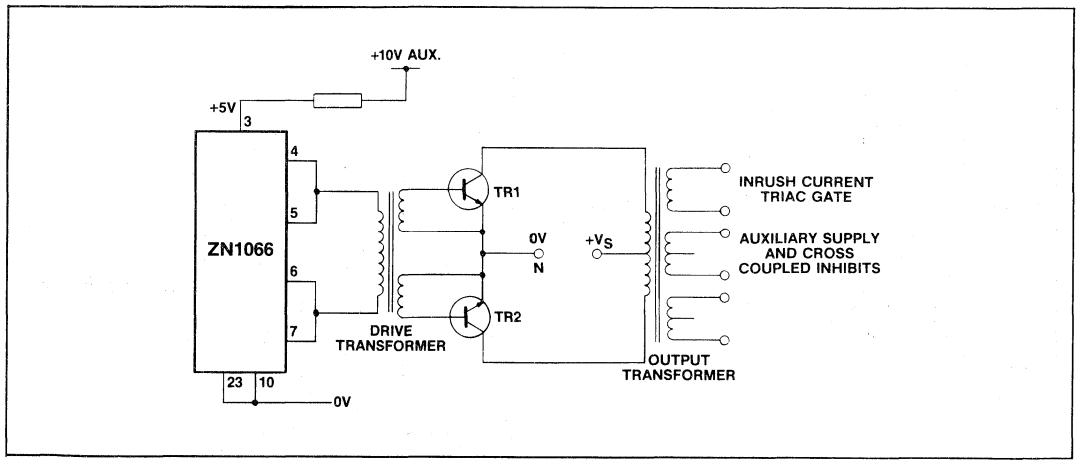


Fig.26 Typical transformer coupled push-pull circuit

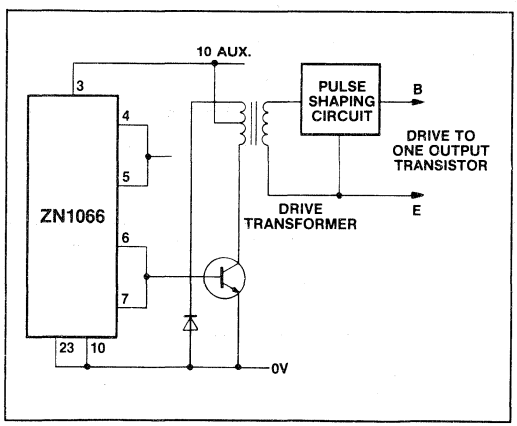


Fig.27 Typical high power high input voltage interface circuit

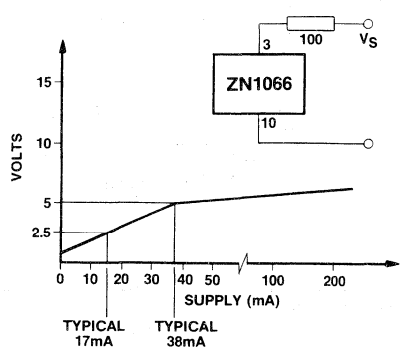


Fig.28 Shunt regulator characteristics

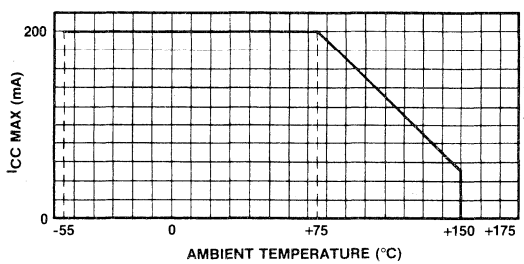


Fig.29 Derating curve (Icc max. Vs ambient temperature)

The advantage of this type of circuit is that it retains the current suck-out capability of the ZN1066 and powers up to 200W are possible. For higher power applications it is necessary to buffer the output from the ZN1066. Fig.27 outlines a common method of interfacing.

5V SHUNT REGULATOR

The total supply current to the ZN1066 is divided between three main functional areas:

(a) Internal Control Circuitry

(b) Average output load currents

(c) 5V shunt regulator

Since the control circuits are fed from the 5V stabilised supply rail, the current drawn is independent of external conditions over the operating range of the shunt regulator. Fig.29 shows a typical plot of the stabilised supply versus input in the absence of output loads. The supply current at the knee of the characteristic was approximately 35 to 40mA for the sample tested.

In order to keep the total package dissipation to a minimum in a particular application the supply current should be tailored to suit the output drive requirements. Current in excess of this will be carried by the shunt regulator.

Assuming an operating duty cycle of nominally 50% a suitable current would be: Peak output current + 40mA. See Fig.29 for temperature operating.

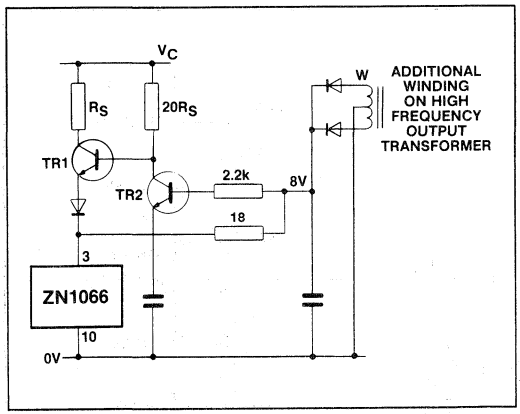


Fig.30 Start up circuit

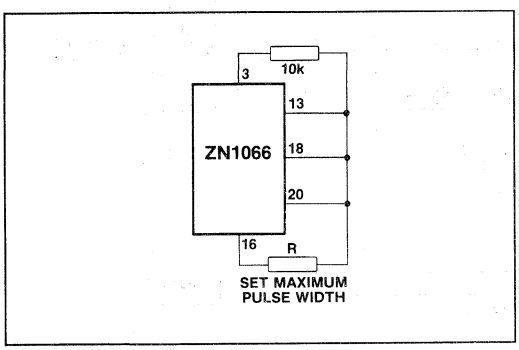
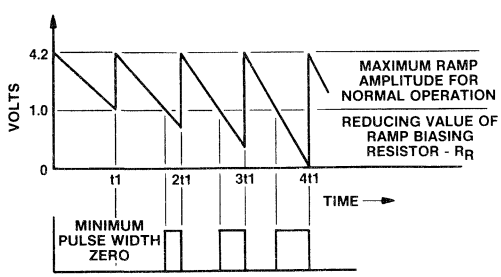


Fig.31 Presetting maximum pulse width



Minimum pulse width increasing with reduced value of ramp biasing resistor R_R.

Fig.32 Presetting minimum pulse width

AUXILIARY SUPPLY

In some applications it may be advantageous to derive the initial power for the ZN1066 from the main supply, Vs via a start circuit. One method of achieving this is illustrated in Fig.30.

Initially, current for the ZN1066 is provided via Rs and TR1; TR2 is not conducting. When the output from the additional winding on the high frequency transformer is large enough the current required by the ZN1066 is provided via the 18Ω resistor. When steady-state conditions have been established transistor TR2 bottoms and shuts off TR1. The operation of the start circuit is inhibited, and there is little further dissipation in it.

OUTPUT PULSE WIDTH SETTING

Tt pulse width is infinitely variable from 0 to 50%, mode control at 0V, or 0 to 100% mode control at +5V.

The maximum pulse width can be preset to any desired value by simply connecting a resistor of suitable value between pins 13 and 16 as indicated in Fig.31.

The minimum pulse can also be preset to any desired value by adjusting the value of the ramp biasing resistor R_R connected to pin 11 (see Fig.3). The function of this is illustrated in Fig.32.

TYPICAL CIRCUITS

Fig.33 illustrates a 120VA direct coupled push-pull power supply. Input/output isolation is achieved by means of the voltage tracking opto-isolator circuit previously described in Fig.14. The design also incorporates the essential soft start circuit to prevent damage to the power transistors on turn-on and current limit is by sensing the transistor collector currents as previously described. The transistors are also protected against simultaneous conduction by means of the cross coupled inhibits, pin 1 and pin 2.

Fig.34 illustrates a 100VA push-pull switched mode power supply. The design incorporates soft start, foldback current limiting protection against cross current conduction and a controlled start-up.

This circuit is easily modified to include current limit on the primary side by using the cycle-by-cycle current limit described in Fig.13. Alternatively if output current sensing is not required the on-chip current control amplifier can be used to provide a constant current characteristic based on sensing the switching transistor collector currents. One method of achieving this is shown in Fig.12.

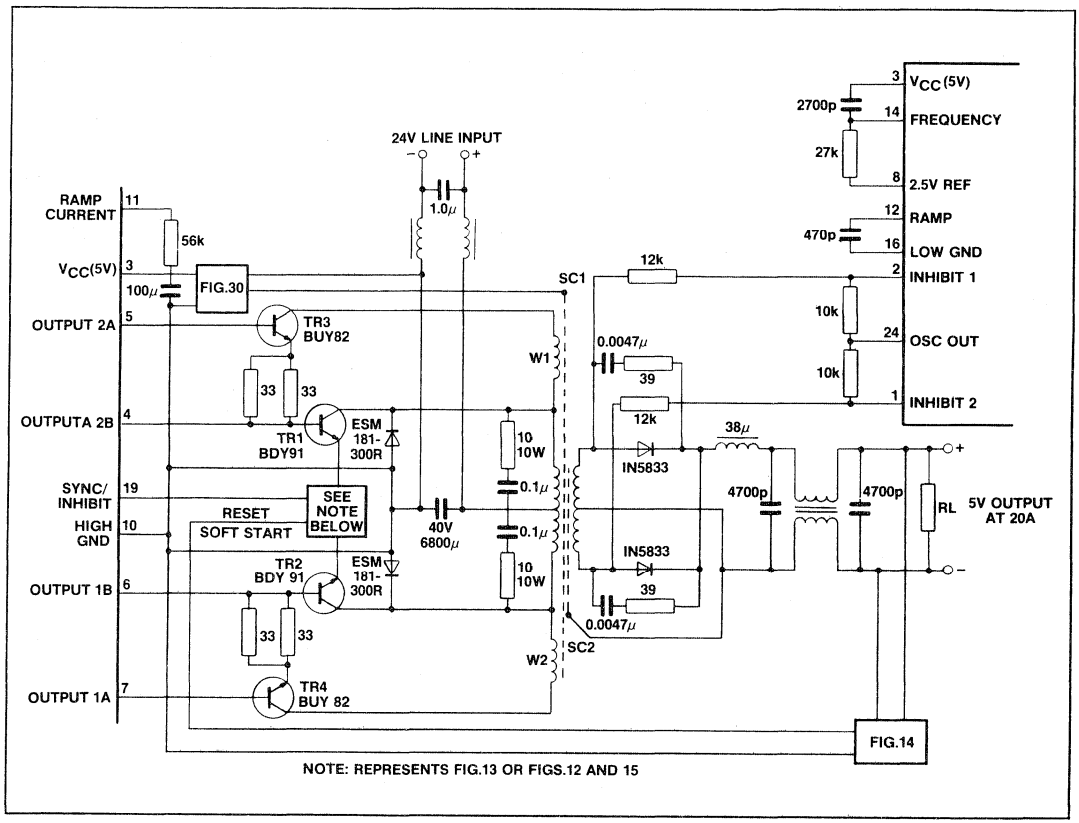


Fig.33 120VA DC/DC converter

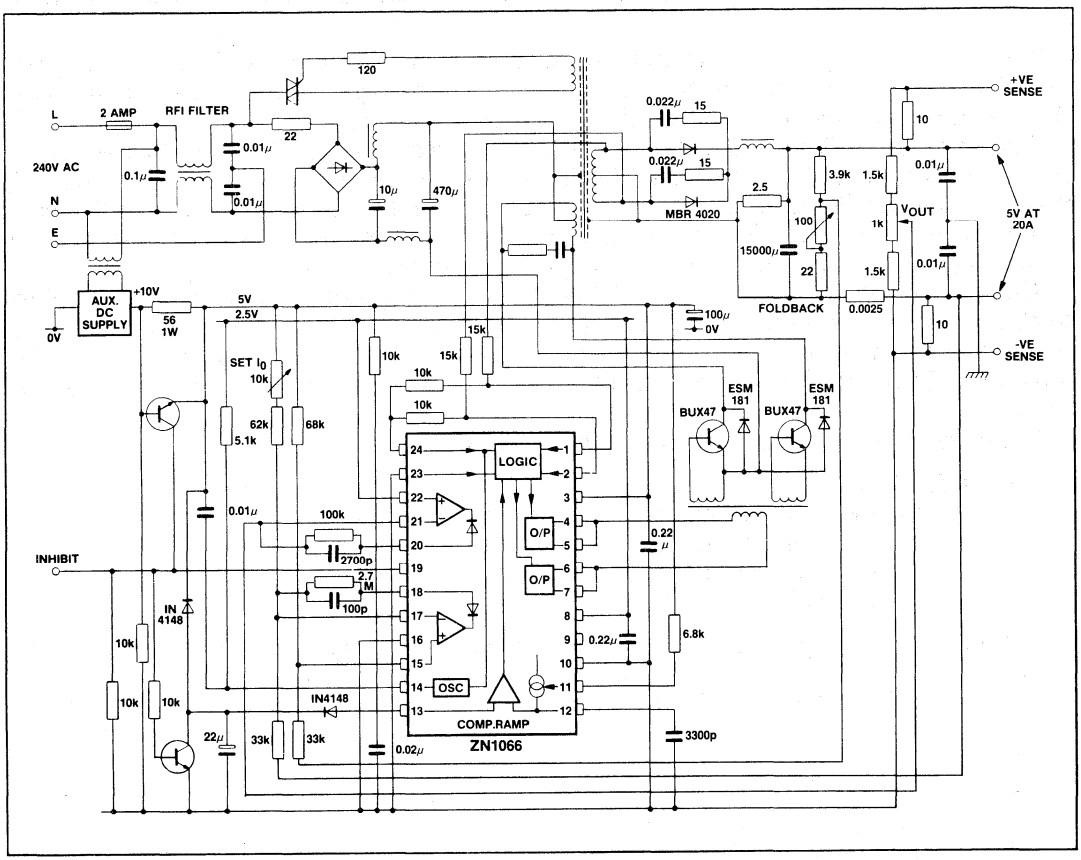


Fig.34 100VA off line SMPSU

Thermal Design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{ja} = \theta_{jc} + \theta_{ch} + \theta_{ha}$

where θ_{ja} is thermal resistance junction-to-ambient °C/W
θ_{jc} is thermal resistance junction-to-case °C/W
θ_{ch} is thermal resistance case-to-heatsink °C/W
θ_{ha} is therrnal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{ja})$
T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

A device is to be used at an ambient temperature of +50° C. θ_{ja} for the DG14 package with a chip of approximately 1mm sq is 107° C/W. Assuming the datasheet for the device gives P_D = 330mW and T_j max = 175° C.

$T_j = T_{amb} + P_D \theta_{ja}$
$= 50 + (0.33 \times 107)$
$= 85.31°C$ (typ.)

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Example 2

A device with T_{amb} max. = +175° C is to be used at an ambient temperature of +150° C. Again, θ_{ja} = 107° C/W, P_D = 330mW and T_j max. = +175° C.

T_j = 150 + (0.33 x 107)
= +185.3° C (typ.)

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{ja} is the sum of the individual thermal resistances; of these, θ_{jc} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{ca}, can be reduced.

If θ_{ca}, and therefore θ_{ja}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{ja} of 55° C/W for the DG14 package. Using this heatsink with the device operated as in Example 2 would result in a junction temperature given by:

T_j = 150 + (0.33 x 55)
= 168° C

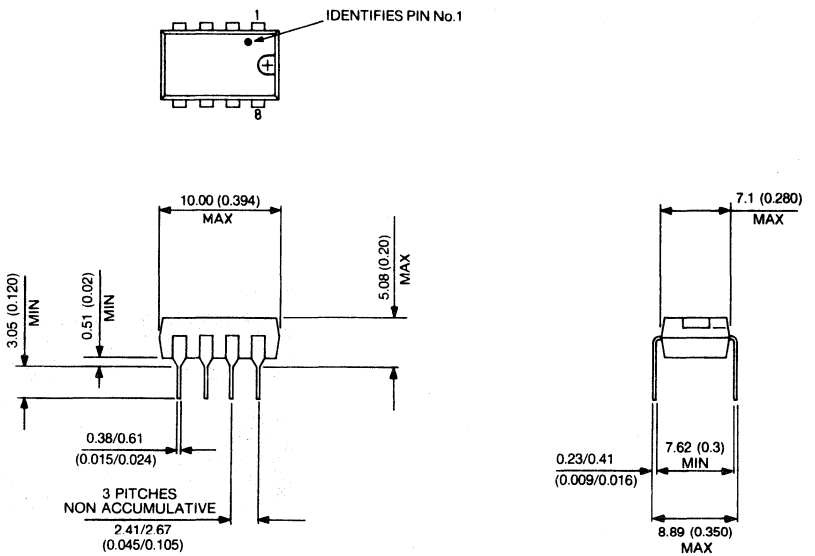
Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{jc} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{jc} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

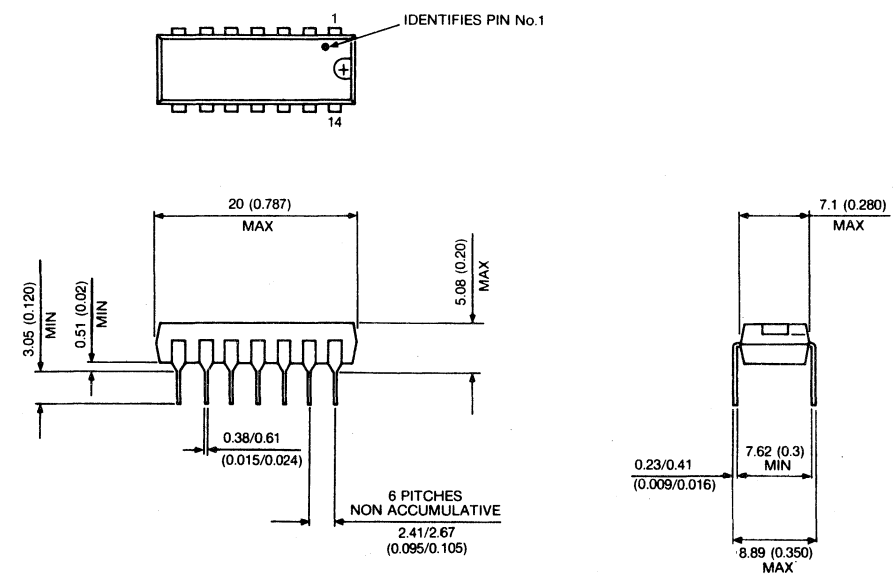
It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

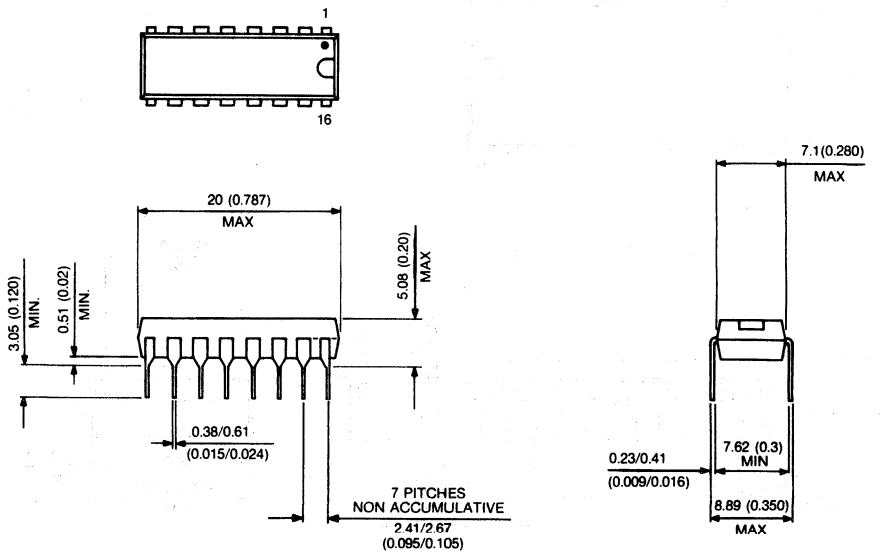
Package Outlines



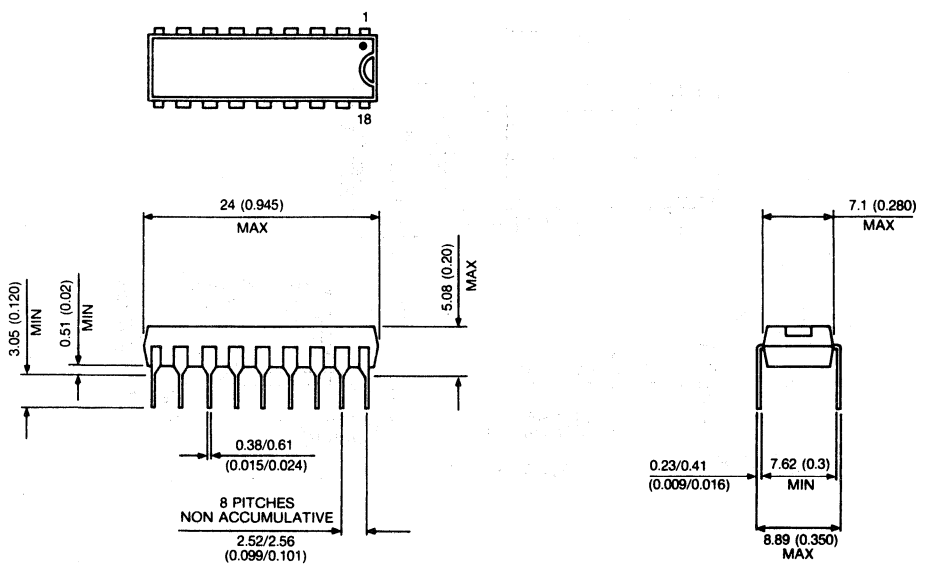
8-LEAD PLASTIC DIL - DP8



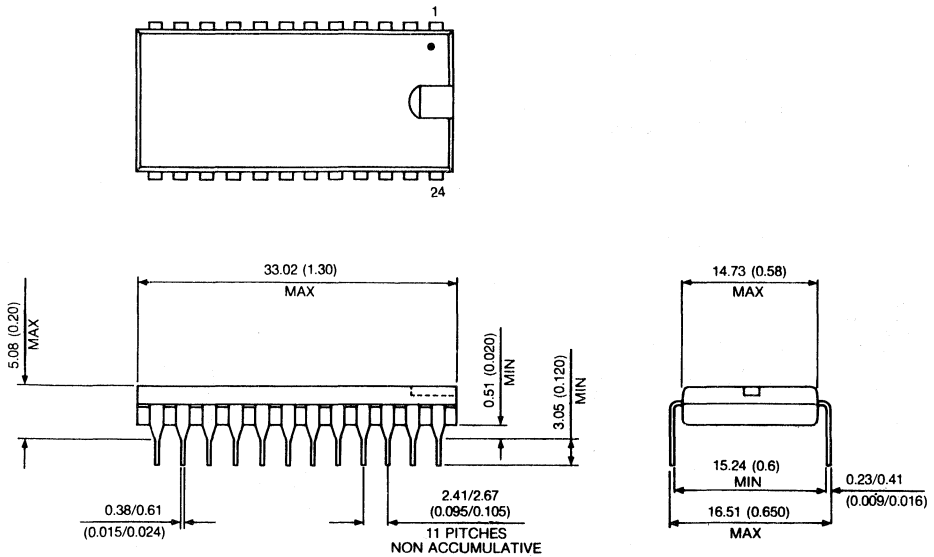
14-LEAD PLASTIC DIL - DP14



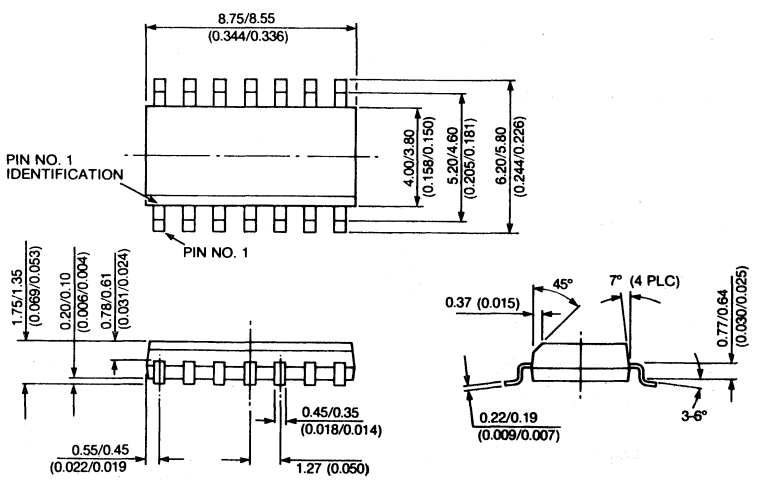
16-LEAD PLASTIC DIL - DP16



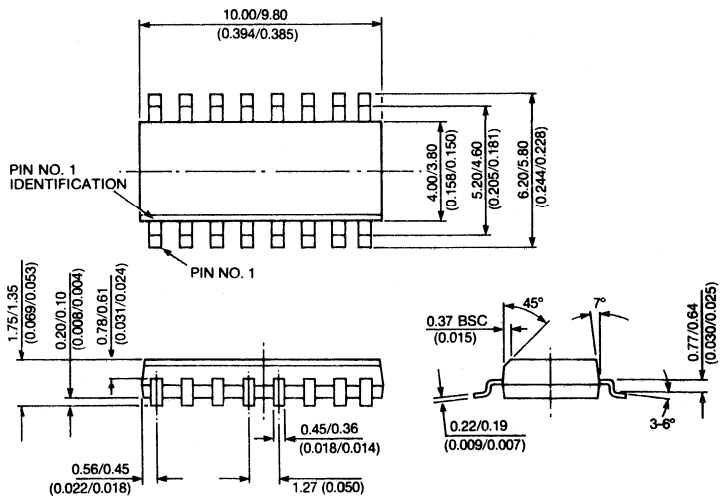
18-LEAD PLASTIC DIL - DP18



24-LEAD PLASTIC DIL - DP24



14-LEAD MINIATURE PLASTIC DIL - MP14



16-LEAD MINIATURE PLASTIC DIL - MP16

Stop Press

PLESSEY
Semiconductors

ZN1036E/D

PROGRAMMABLE COUNTER TIMER INTEGRATED CIRCUIT

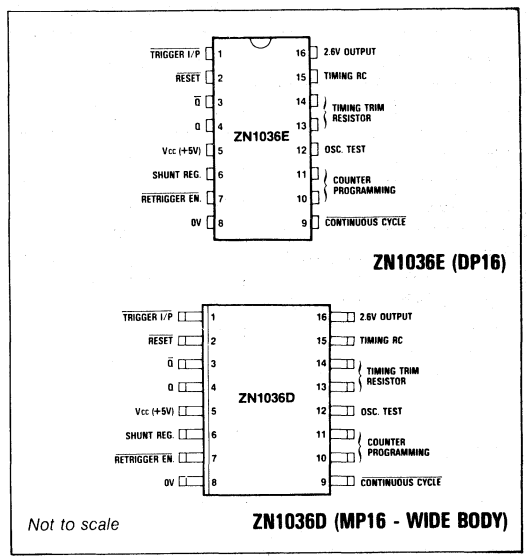
The ZN1036 combines linear and digital functions on the same chip such that simple precision timers can be constructed using the minimum of low cost external components. The frequency of an on-chip oscillator is determined by an external capacitor and resistor. Fine adjustment can then be achieved by the variation of an external trimming resistor. A buffered oscillator output can be used to monitor the trimming operation without affecting the oscillator frequency.

Pulses from the oscillator are fed into a programmable counter and the output changes state after a preset number of pulses. The counter is programmable in 4 stages - 4095, 2047, 1023 and 511 counts.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller value than would be required by single RC time constant timers.

The count can be initiated either (a) with trigger input LO and supply going HI (supply initiation), or (b) with supply HI and trigger input going LO (trigger initiation). The timer can also be retriggered at any point (thus initiating a new timing period) or reset, terminating the time period.

The IC can operate from normal +5V logic supplies or from any higher voltage using a dropping resistor and internal shunt regulator connected to the supply pin.



Pin connections (top view)

FEATURES

- External Control of Operational Mode
- Accurate and Repeatable Performance
- Complementary High Current Output Drivers
- Buffered Oscillator Output for Easy Oscillator Calibration
- Time Period Trimming
- Supply or Trigger Input Timing Initiation
- Continuous Cycle Facility
- On-Chip Regulator or TTL Supply Option
- Minimum of External Components Required
- Available in Plastic DIL (DP) — ZN1036E and Miniature Plastic DIL (MP) — ZN1036D

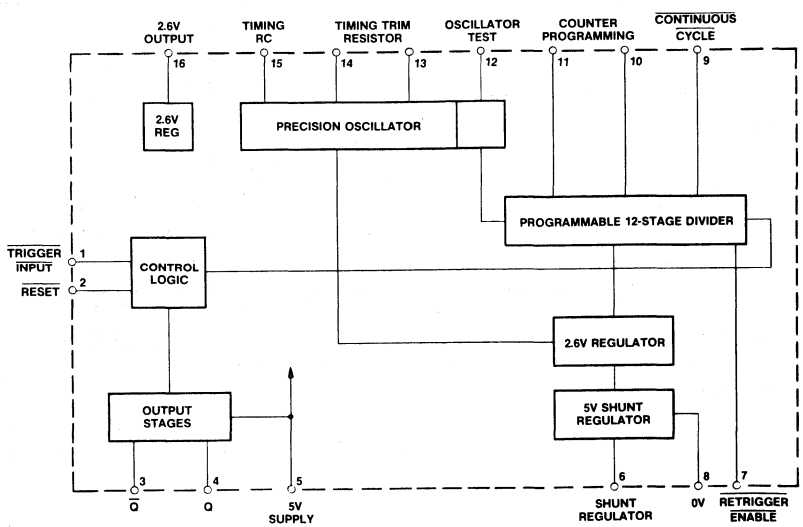


Fig.1

ABSOLUTE MAXIMUM RATINGS

Dissipation	250mW derate above 30°C at 5mW/°C
Output source current	25mA
Output sink current	25mA
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Timing section						See Note 5
Timing resistor	R_T	2k7		5M6	Ω	
Timing capacitor	C_T	0.1			nF	See Fig 2
Trim resistor	R_{trim}	0		560	kΩ	
Repetitive timing error			0.01		%	
Timing initiation and reset						
(a) Supply voltage initiation						
Voltage to initiate timing	V_{CC}	4.7			V	supply applied to pin 5 with Pin 1 connected to Pin 8
Rate of change of V_{CC}				0.25	V/μs	
(b) Trigger input initiation						
Voltage to initiate timing	$V_{T(LO)}$			1	V	
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) Supply voltage reset						
Voltage to reset	V_{CC}		3.6		V	See note 2
External clock input						
Frequency				250	kHz	Clock input to pin 14 via a 10k resistor
Drive current	I_{clk}		0.1		mA	
Pulse width	t_{clk}	2			μs	
Pulse amplitude	V_{clk}	2.5		5.5	V	

Parameter	Symbol	Conditions	
Time multiplying factor	M	Pin 10	Pin 11
4095		H	H
2047		H	L
1023		L	H
511		L	L

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply						Note 4
(a) Externally regulated						connected to Pin 5
Supply voltage Supply current	V_{CC} I_{CC}	4.5	3.8	5.5 4.5	V mA	V_{CC} = 5V outputs unloaded
(b) Internally regulated (5V shunt regulator)						connect pin 5 to Pin 6. Note 4
Operating current range	I_R	5		55	mA	see Note 3
Regulated voltage	V_R	4.5		5.5	V	I_R = 10mA
Slope resistance			1.25		Ω	I_R = 7 – 55mA
Regulated voltage change with temperature			35		mV	I_R = 7 – 55mA t = 0 to +70°C
(c) Reference voltage (2.5V series regulator)						
Regulated voltage	V_{REF}	2.4	2.5	2.6	V	V_{CC} = 5V, Pin 16 unloaded
Load current	I_{REF}		1		mA	V_{CC} = 5V
Slope resistance			2.5		Ω	
Output drive Q to $\overline{Q}$						V_{CC} = 5V
Output voltage	$V_{O(HI)}$ $V_{O(LO)}$	2.5 0.3	3.0 0.4	3.2 0.6	V V	$I_{O(HI)}$ = 25mA $I_{O(LO)}$ = – 25mA
Output current	$I_{O(HI)}$ $I_{O(LO)}$			– 25 + 25	mA mA	Source Sink
Rise time	t_r		300		ns	I_O = 5mA, V_{CC} = 5V
Fall time	t_f		100		ns	I_O = 5mA, V_{CC} = 5V
Propagation delay V_T Low to V_O High	t_p		2.3	2.5	μs	
Oscillator test output swing		3	4	5	V	10k Pull up to 5V
Temperature coefficient	T_C		0.008		%/°C	R_{TRIM} = 56k

Note 1 Time = MCR

C = capacitance in μF
R = resistance in MΩ
M = multiplying factor

For $t_{osc} \geqslant 10\mu s$

At $t_{osc} < 10\mu s$ this relationship no longer holds as the reset time becomes a significant fraction of t_{osc}

Ncte 2 In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically acheived at 3.6V. Reset will not occur with the supply greater than 4V

Note 3 Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 4.5mA maximum supply current taken by the timer.

Note 4 A 0.1μF capacitor should be connected between V_{CC} (Pin 5) and G_{ND} (Pin8) at all times.

Note 5 Minimum recommended oscillator period = 4μs

SECTION 1 THE TIMING FUNCTION

1.1 Fixed time period

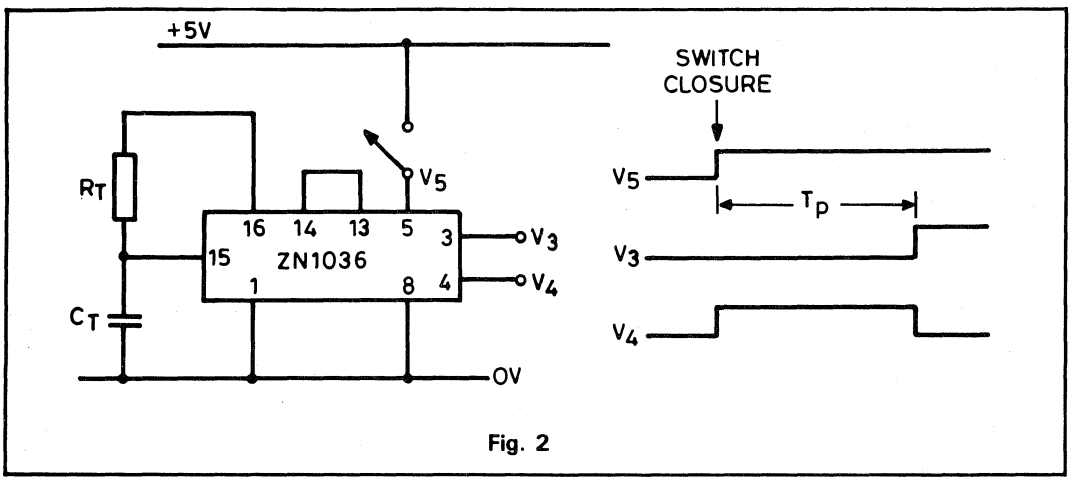


Fig. 2

External components R_T and C_T determine the length of period T_p. The timing components set the period of an internal oscillator to C_T R_T ±10% and an internal divider causes a change in the output state after a preset number of oscillator cycles (determined by counter programming Pins).

When the time period is initiated Pin 4 goes Hi for a time period T_p. On completion of the time period, Pin 4 goes Lo and Pin 3 which was previously Lo goes Hi and remains Hi until the timing sequence is re-initiated.

1.2 Trimming the time period

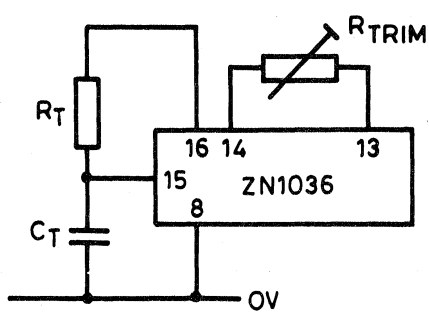


Fig. 3

1.3 Design of variable period timers

Time periods from 2.044ms to infinity may theoretically be obtained using the ZN1036 integrated timer circuit. The following section should enable the designer to get the best possible circuit configuration achievable within the design limits. The necessary information is presented below, Fig 4, in the form of a timing components against oscillator period graph. The graph has been plotted using a 56kΩ trim resistor between Pins 13 and 14.

The maximum range of oscillator period possible for a particular value - or timing capacitor can easily be obtained from the graph. To obtain the time period the oscillator period (from Fig. 4) is multiplied by the multiplying factor M (determined by programming Pins 10 and 11)

The periods obtained with the timing components selected from Fig. 4 may be trimmed to the exact time required using a variable resistor up to the value of 560kΩ between Pins 13 and 14.

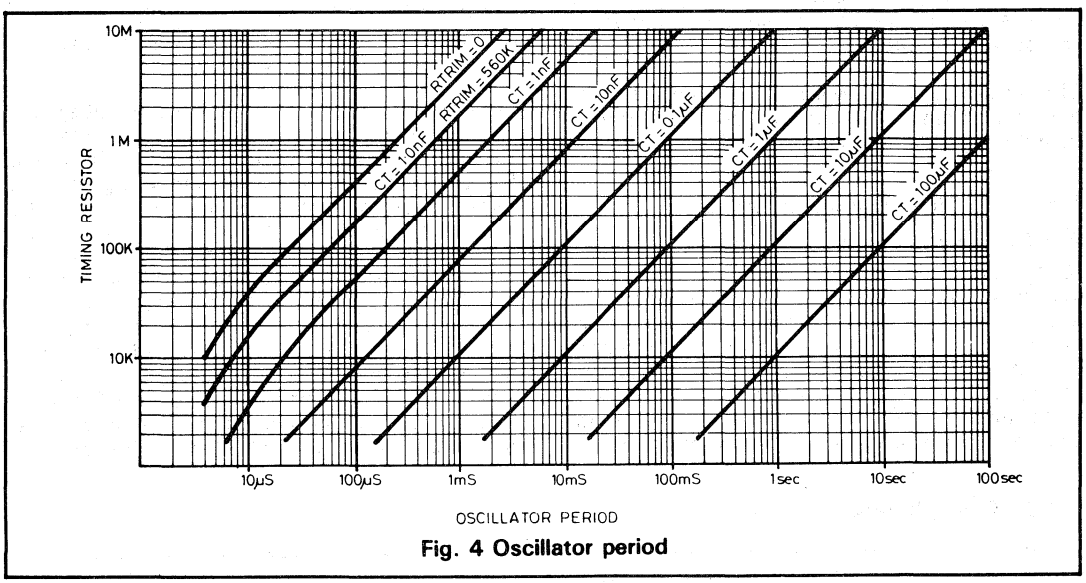


Fig. 4 Oscillator period

SECTION 2 INPUT AND OUTPUT CIRCUITS

Note 2.1 External clock

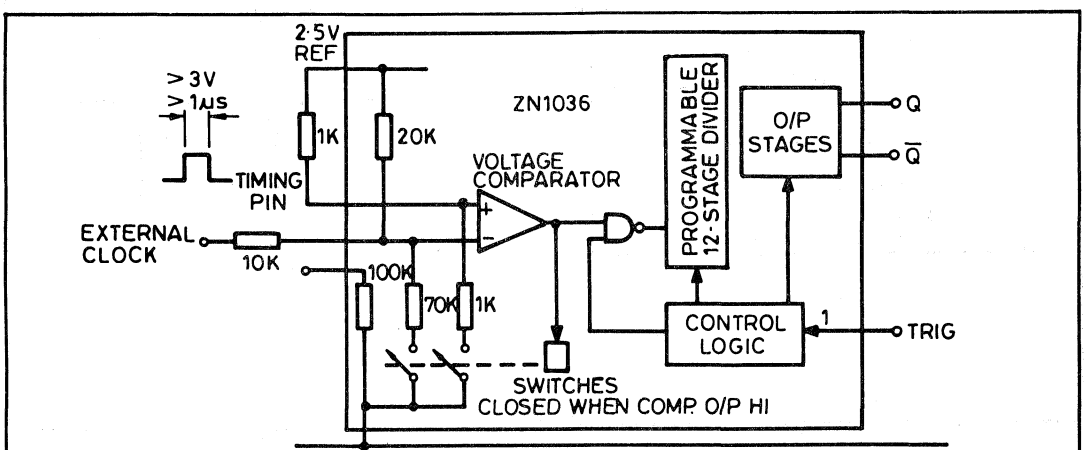


Fig. 5

The ZN1036 can be used with an external clock as shown in the circuit of Fig. 5.

The internal clock is disabled by connecting a 1k resistor from the timing pin 15 to the +2.5V reference pin 16 thus preventing the non-inverting i/p to the amplifier dropping below the inverting input voltage. The amplifier output is therefore HI and the internal switches are closed.

An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on pin 15 and, if the trigger i/p on pin 1 is LO, will cause a pulse to be passed to the divider circuit.

The output Q and $\overline{Q}$ will change from LO to HI and vice versa at the end of a present number of external clock pulses.

Note 2.2 Timing initiation and reset

2.2.1 Supply initiated

When pin 1 is held 'LO' and the supply is switched on, the control logic and counters are automatically reset as the supply rises to its on voltage. This also initiates timing at the same instant by gating the oscillator output into the counter. After the set time the outputs change state and remain thus until the supply is switched off or another period is initiated.

If, during such a timing cycle the trigger input is taken HI, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. If the supply drops below the reset level even for a few microseconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period. The timer can also be reset at any time by taking Pin2 Lo.

2.2.2 Trigger initiated

Allowing pin 1 to rise with the supply prevents timer initiation by the supply.

Pulling the trigger input 'LO' now initiates a normal timing period. A further period may be initiated by dropping the trigger LO again. This period is not affected when the trigger input level is altered during timing - as long as the 'retrigger enable' (Pin 7) remains Hi. When the retrigger enable goes Lo during timing any further trigger pulse will cause the initiation of a further time period at that point. The period is terminated again by the supply falling below the reset level or a Lo pulse to reset Pin 2. Since the normal condition of the trigger is Hi the timing will not restart on restoration of supply. A supply drop-out during a trigger initiated timing period has the effect of shortening the set time.

2.2.3 A simple repetitive timer

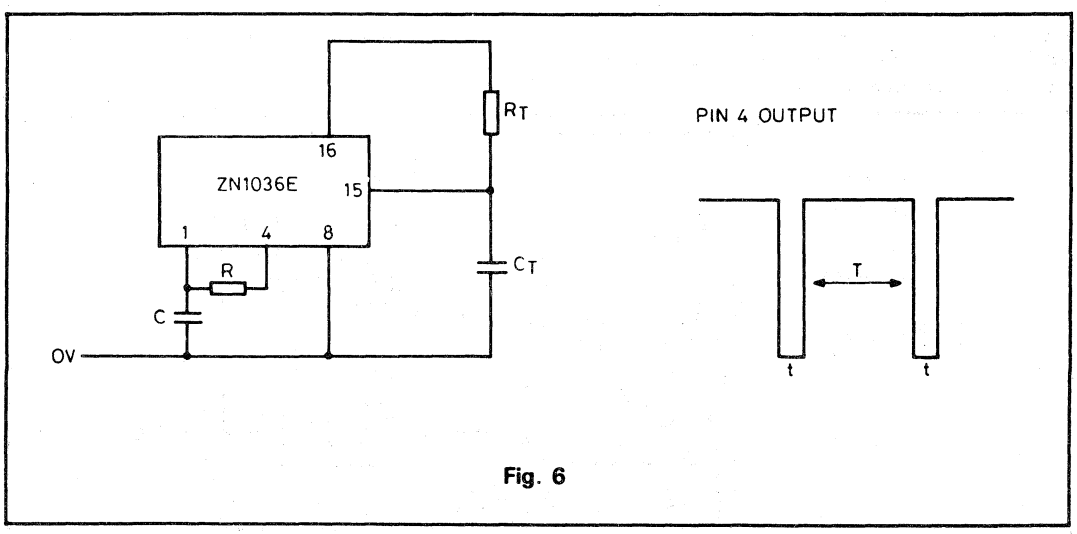


Fig. 6

A capacitor and resistor in the feedback loop can be used and the pulse length t determined by the values of C and R. T is determined by timing components R_T and C_T. R may be any value up to 10k whilst C is limited to 10μF.

2.2.4 A simple closed loop timer

The ZN1036 enables the designer to construct multistage timers with ease as one can be triggered by a single wire link from the output of another.

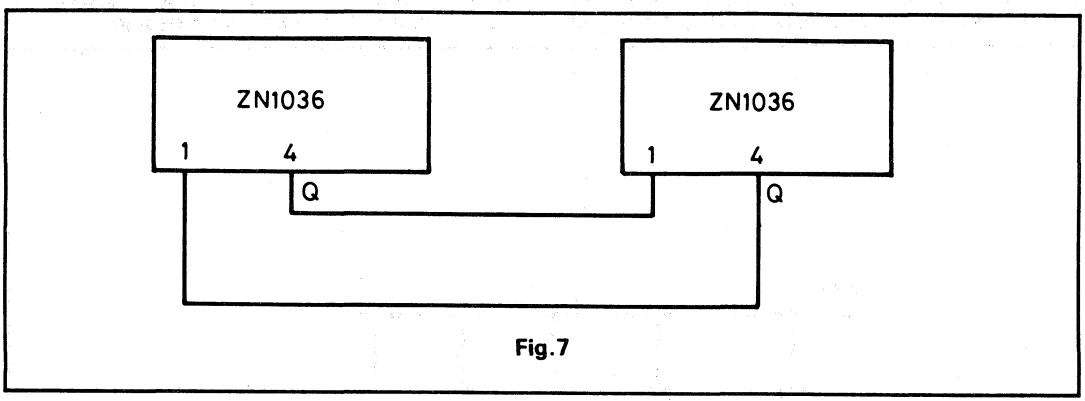


Fig.7

This may in theory be extended to any number of counters but for more than 3 there will be other modes of oscillation. For a ring of three, component tolerances will usually ensure that one mode is dominant with only one Q output Hi at a time. Higher numbers may not operate in the desired mode unless one set time is greater than the sum of all the others.

Fig. 8 shows a four stage ring timer.

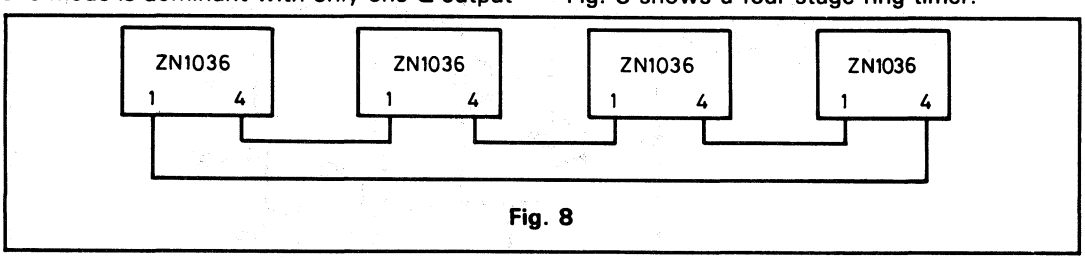


Fig. 8

2.2.5 ZN1036 Waveforms

The function of this device is demonstrated below as a Waveform diagram (Fig. 9)

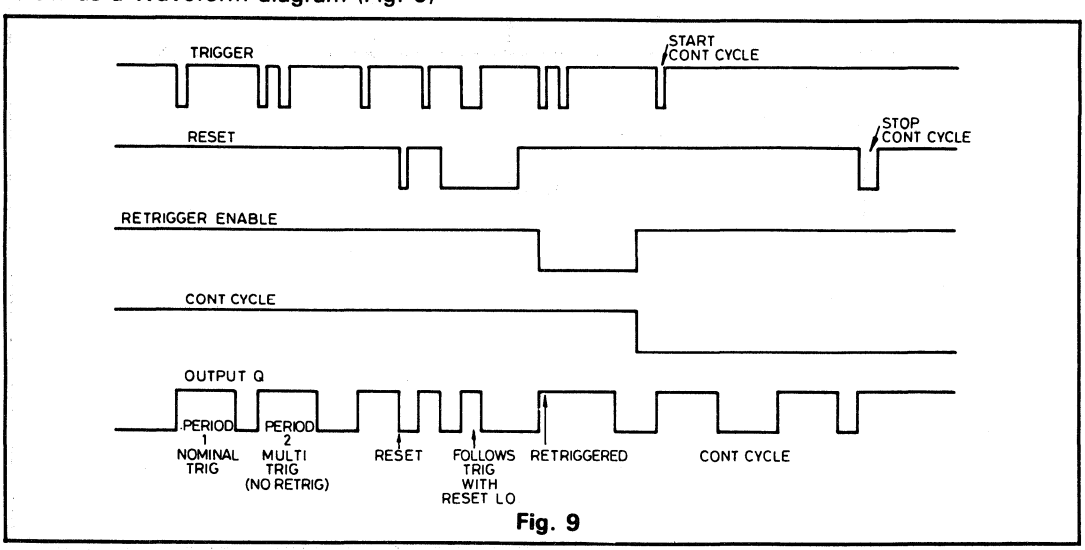


Fig. 9

2.3 Trigger input circuit

The input circuit comprises of a buffer input followed by a schmitt trigger circuit. The buffer pull up resistor can be as low as 30kΩ. So to pull the input down below the IV threshold a pull down resistor of less than 5.6kΩ is recommended for worst case design.

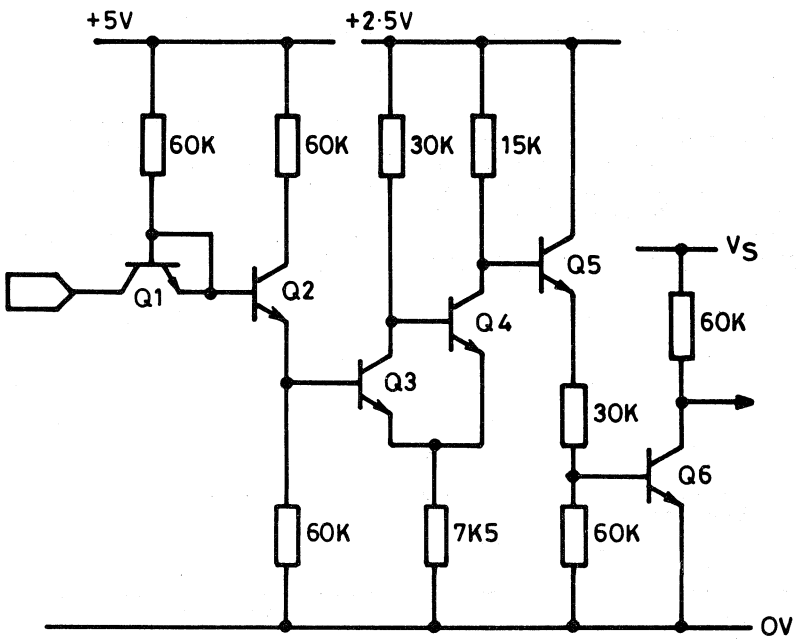


Fig. 10

2.4 Output drive circuits

The Q and $\overline{Q}$ output drive circuits have the form illustrated in Fig. 11

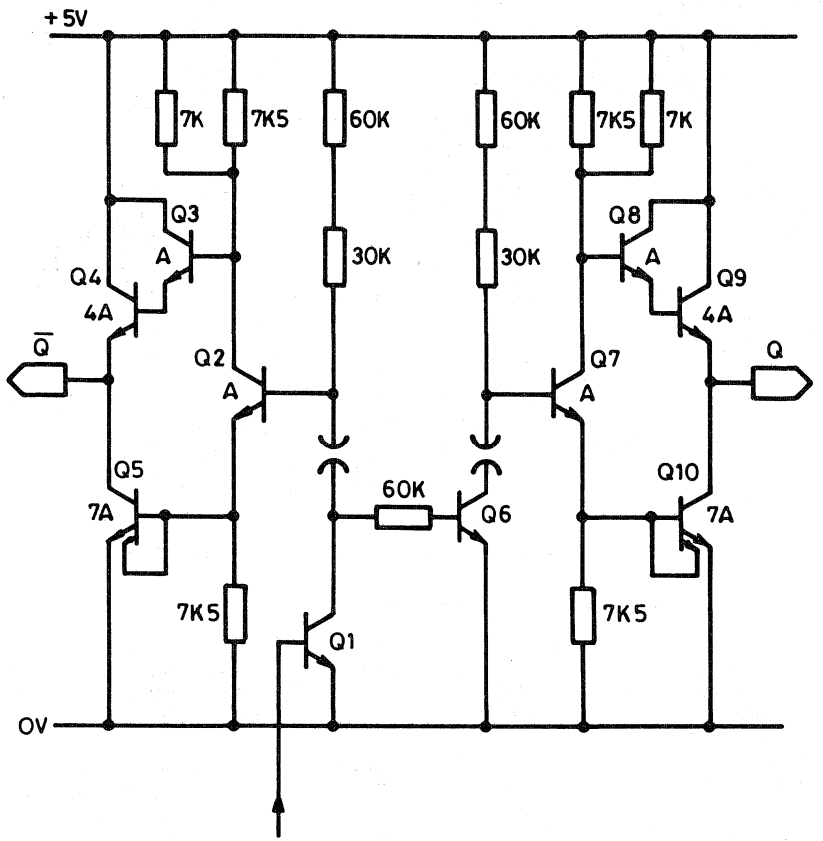


Fig. 11

2.5 Load circuits

2.5.1 Transistor driven relay

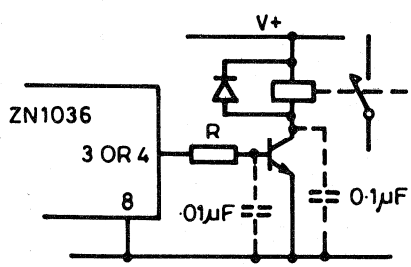


Fig. 12

The value of R is chosen to limit current to minimum required by the transistor under the worst condition.

If interference is experinenced suppression capacitors as shown may be needed.

2.5.2 Thyristor driven relay

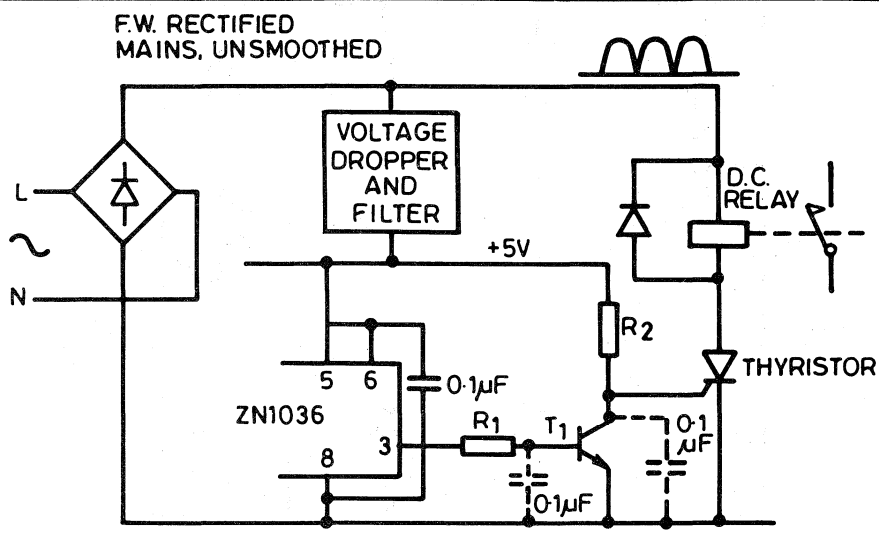


Fig. 13

A thyristor gate may be driven via a limiting resistor directly from pin 3 for DELAY-TO-ON timers. Fig. 13 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_1) just reaches saturation.

For 240 volts a.c. mains it may be necessary to use a 110 volt d.c. relay with a dropping resistor of equal resistance since 220 volts d.c. relays are not easily obtainable.

2.5.3 Triac a.c. load circuit positive firing

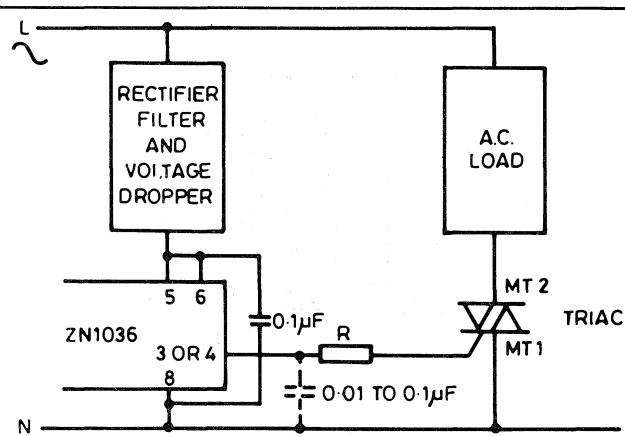


Fig. 14

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

2.5.4 Triac a.c. load circuit negative firing

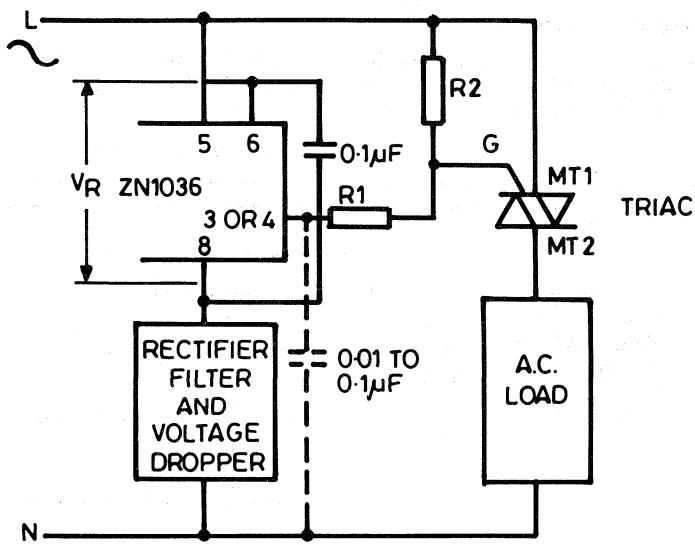


Fig. 15

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the 1036 output drive voltage is a maximum since the total output swing would be $V_{R\ Min} - V_{O(LO)\ Max} \simeq 4.3$ volts for a current of 25mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1036 outputs than would be the case for positive firing circuits.

2.5.5 Output state indication

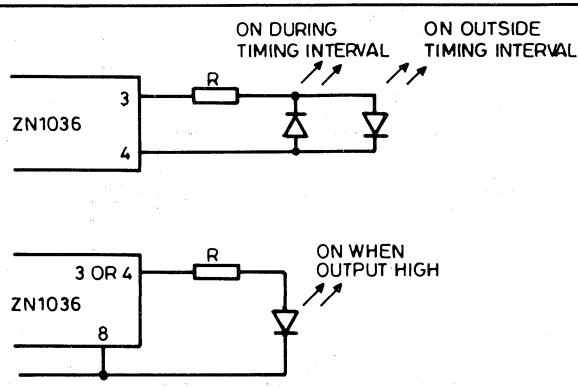


Fig. 16

The value of R is chosen to limit the current to the LED requirements. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs.

SECTION 3 POWER SUPPLIES AND REFERENCES

3.1 Externally regulated supplies

If a 5V ±10% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 6 unconnected the minimum current drain of 2mA required is avoided. The current available from the supply should not fall below a level of:

$$I_{CC} = (5mA + \text{the output current from pins 3 or 4})$$

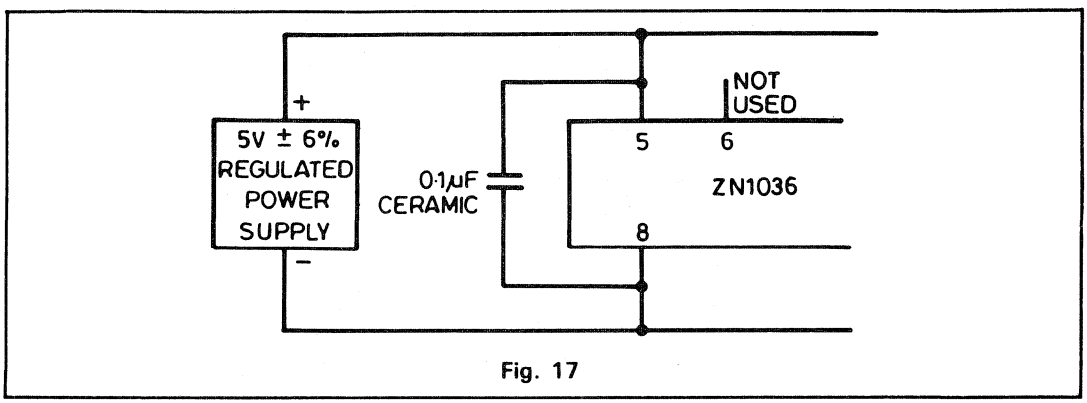


Fig. 17

N.B. The supply should be decoupled by 0.1μF capacitor connected as close as possible to pins 5 and 8.

3.2 Internally regulated supplies

3.2.1 d.c. supplies greater than 5 volts

By connecting pin 6 to pin 5 an on-chip shunt regulator allows the use of unregulated d.c. supplies higher than 5 volts. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V and ±25% is shown below.

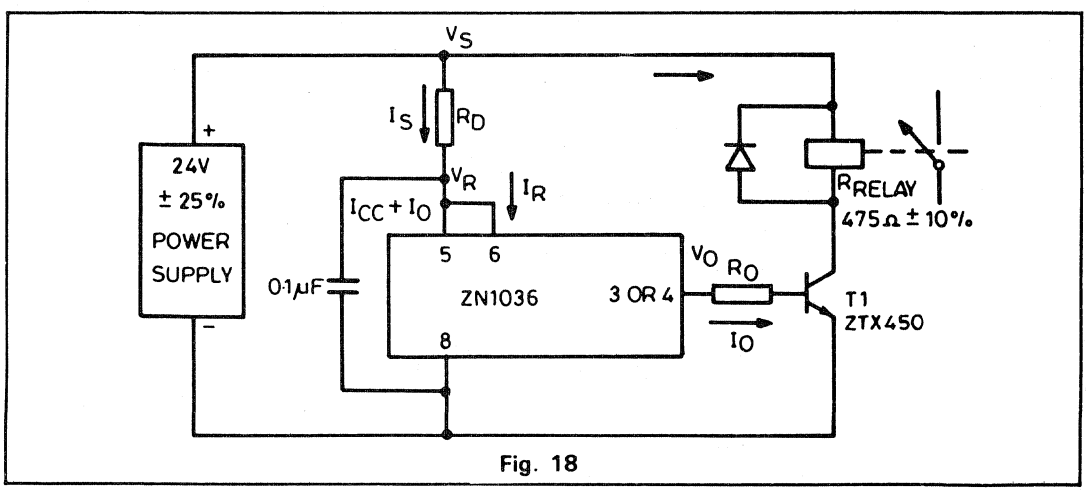


Fig. 18

N.B. The supply decoupling capacitor also acts as stabilisation for the internal regulator and the connection between pins 6 and 5 should therefore be as short as possible.

The values of R_O and R_D used in the circuit of Fig. 18 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of T_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24(+25\%)}{475(-10\%)}$$

$$= \frac{1}{50} \cdot \frac{30}{427}$$

$$\mathbf{I_{O(Min)}} = \mathbf{1.4mA}$$

Deriving $V_{O(Min)}$ for the output circuit (Fig. 11)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)}} = \mathbf{3.3\ volts}$$

Hence $$R_O = \frac{3.3 - V_{BE\,T_1}}{1.4}\ k\Omega \quad (V_{BE\,T_1} = 0.6V)$$

$$= 1.9k$$

Choose $$\mathbf{R_O} = \mathbf{1.8k}\ \text{(Nearest lower preferred value)}$$

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above $$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$\mathbf{V_{O(Max)}} = \mathbf{3.9\ volts}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE\,T_1}}{1.8} = 1.8mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 1 + 1.8$$

$$\mathbf{I_{S(Min)}} = \mathbf{8.8mA}$$

Hence $$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$

$$= \frac{18 - 5.3}{8.8}\ k$$

$$\mathbf{R_D} = \mathbf{1.5k}\ \text{(Nearest preferred value)}$$

The power dissipated in the dropping resistor and the ZN1036 can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k(-5\%)}$$

$$= \frac{30-4.7}{1.425}\ mA$$

$$I_{S(Max)} = \mathbf{18mA}$$

Hence the ZN1036 dissipation $= \underline{90mW}$ max. and power dissipation by dropping resistor $= \underline{450mW}$ max.

The calculations assume $\pm 2\%$ tolerance resistors.

3.2.2 a.c. mains supplies

A transformer may be used to drop the voltage from the mains and a rectified d.c. supply provided as discussed in 3.2.1

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of a.c. or d.c. higher than 5 volts. With a load such as the directly driven triac (sections 2.5.3 and 2.5.4) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the I.C. supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

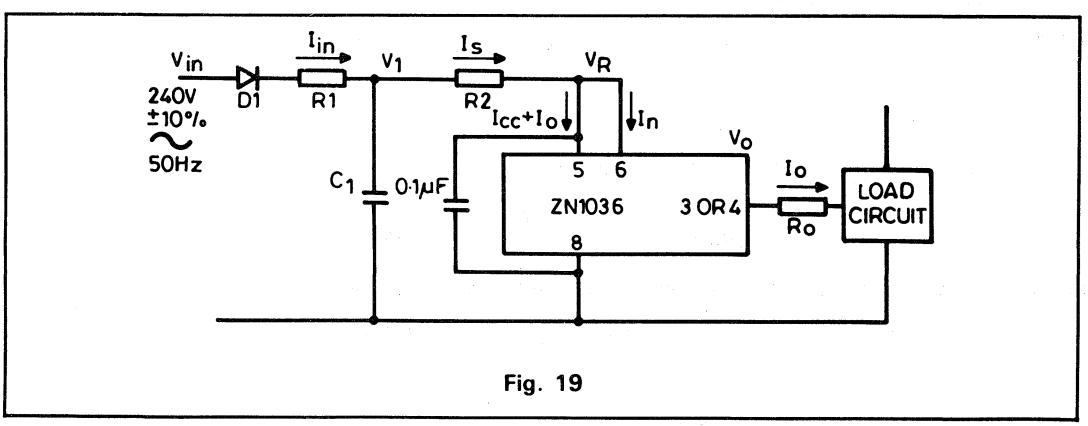


Fig. 19

The value of R_O and $I_{O(Max)}$ are calculated as in 3.2.1 and as an example a current $I_{O(Min)}$ of 10mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore

$$V_{O(Min)} = \mathbf{3.3V}$$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}}\ \Omega\ (V_GT_1 = 2V \text{ for RS } 202)$$

$$R_O = \mathbf{120\Omega}\ \text{(Nearest lower preferred value)}$$

$$V_{O(Max)} = \mathbf{3.9V}$$

Hence

$$I_{O(Max)} = \frac{3.9 - V_G}{0.12}\ mA$$

$$I_{O(Max)} = \mathbf{16mA}$$

And the minimum value of supply current for correct operation is therefore

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$
$$= 5 + 2 + 16$$
$$\mathbf{I_{S(Min)} = 23mA}$$

If we assume that C1 is a 25 volt working capacitor and that 3 volts peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$$V_{1(Min)} = 25(-20\%) - 3 \text{ (Allowing for } \pm 10\% \text{ variation in mains supply)}$$
$$\mathbf{V_{1(Min)} = 17V}$$

Therefore
$$R_2 = \frac{17 - V_{R(Max)}}{23} \text{ k}\Omega$$
$$\mathbf{R_2 = 510\Omega} \text{ (Nearest preferred value)}$$

The current i_{in} will flow for very nearly the full half cycle, 10ms in the case of 50Hz supplies, since V_1 is low compared to the peak mains voltage.

Now
$$i_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$i_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{RIPPLE(avg)} - V_{R(Min)}}{R_2}$$
$$= \frac{17 + 1.5 - 4.7}{510}$$
$$= 27mA$$

Therefore
$$R_1 = \frac{\sqrt{2} \times 240\,(-10\%) - (17 + 1.5)}{\pi \times 27} \text{ k}\Omega$$
$$= \mathbf{3k3} \text{ (Nearest preferred value)}$$

For the required ripple of 3V pk.pk. we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10ms}{3}$$
$$C_1 = \frac{27 \times 10^{-5}}{3}$$
$$\mathbf{C_1} = \mathbf{100\mu F} \text{ (Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $i_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of $$i_{in(avg)} = \frac{V_{in(pk)(Max)} - V_{1(Max)}}{\pi R_1}$$

$$= \frac{2 \times 240\ (+10\%) - 20}{h \times 3.3 \times 10^3}$$

$$\textbf{Max. } i_{in(avg)} = \textbf{34mA}$$

and Max dissipation in $$R_1 = \frac{\pi^2}{4} \times i_{in}{}^2{}_{(avg)} \times R_1$$

$$P_{R1} = \textbf{9.4 watts}$$

When a d.c. load such as the thyristor relay driver of section 2.4.2 is required then a full wave bridge circuit can be used as shown below.

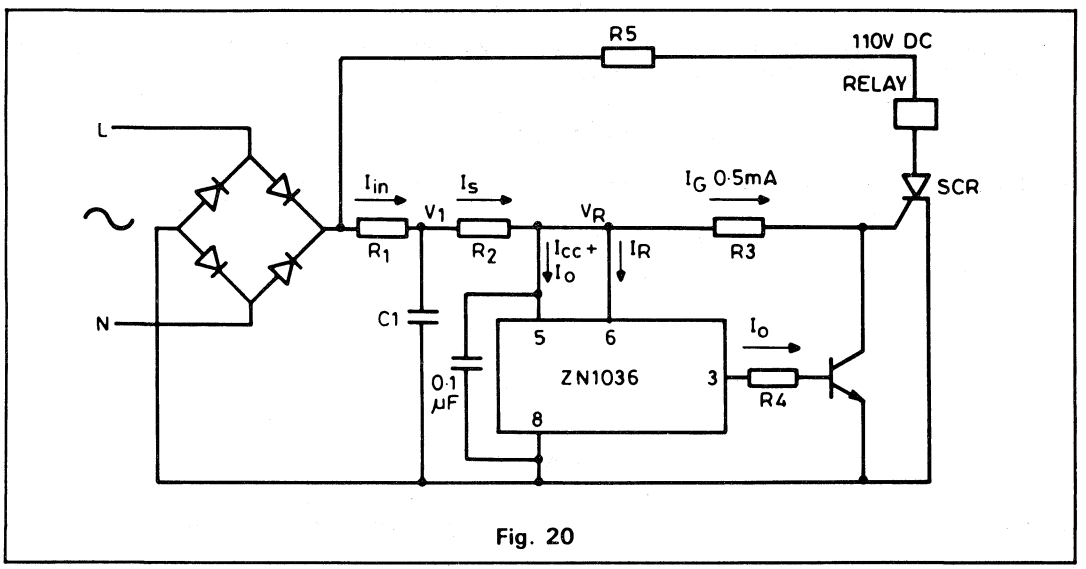


Fig. 20

The DELAY-TO-OFF timer circuit of Fig. 13 has been taken as an example. A typical circuit might have the relay resistance equal to $R_5 = 10k$ and for a 240V ± 10% mains supply the SCR could be a BRX49 which requires less than 0.5mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5mA is sufficient with the above load.

Hence $$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$$

$$= 5 + 2 + 0.5 + 0.5$$

$$I_{S(Min)} = \textbf{8mA}$$

Choosing C_1 to be 25 volts working and 3 volts peak to peak ripple as in the previous example. Then

$$V_{1(Min)} = 25\ (-20\%) - 3$$

$$= \textbf{17 volts}$$

And $$R_2 = \frac{17 - V_{R(Max)}}{8}\ K\Omega$$

$$= \textbf{1.5k} \text{ (Nearest preferred value)}$$

To find the value of C_1 required estimate the angle of conduction. Thus for a sine wave input conduction with change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \text{ Sin } \theta$

and for small values $\theta = \text{Sin } \theta$

Hence $\theta = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2 volt drop across the briage rectifier).

for the rising sine wave $\theta_r = \dfrac{V_{1(Min)} + 1.2}{V_{in(pk)}}$

and for the falling sine wave $\theta_f = \dfrac{V_{1(Max)} + 1.2}{V_{in(pk)}}$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{17 + 20 + 2.4}{305} \text{ (Taking lowest mains input as worst case).}$$

$$= 0.13 \text{ radian}$$

The angle of non conduction $\theta_{tot} \simeq 8°$ and the capacitance will discharge by 3 volts in this period which in terms of time is

$$t = \frac{8}{180°} \times 10\text{ms (for 50Hz mains)}$$

$$= 0.44\text{ms}$$

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)}$ $\qquad (I_{S(Max)} \simeq I_{S(Min)} + 20\%)$

$$\simeq \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3} \ (+20\%)$$

$$\simeq 1.4\mu F$$

So we can choose a $2.2\mu F$ of 25 volt working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{V_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times 305\ 1\ 20}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$\simeq 22\text{k (Next lowest preferred value)}$$

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $i_{in(avg)}$ for the higher limit of the supply.

Maximum value of

$$i_{in(avg)} \simeq \frac{2\,(V_{in\ (pk)\ (Max)} - V_{1(Max)})}{\pi\, R_1}$$

$$= \frac{2}{\pi}\left(\frac{2 \times 240\ (+10\%) - 20}{22 \times 10^{-3}}\right)$$

$$i_{in(avg)} = \mathbf{10mA}$$

Hence

$$P_{R1} = \frac{\pi^2}{8} \times \mathbf{10^{-4}} \times \mathbf{22} \times \mathbf{10^3}$$

$$P_{R1} = \mathbf{2.7\ watts}$$

The calculations have been performed using the 235V ± 10% 50Hz mains figures. Similar calculations may be done for 110V 60Hz or whatever supplies are available.

Note 3.3 Reference supply

The 2.6V reference on pin 16 may be used for an external reference other than for the timing components.

SECTION 4 INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, and timer design illustrated in Figs. 21 and 22.

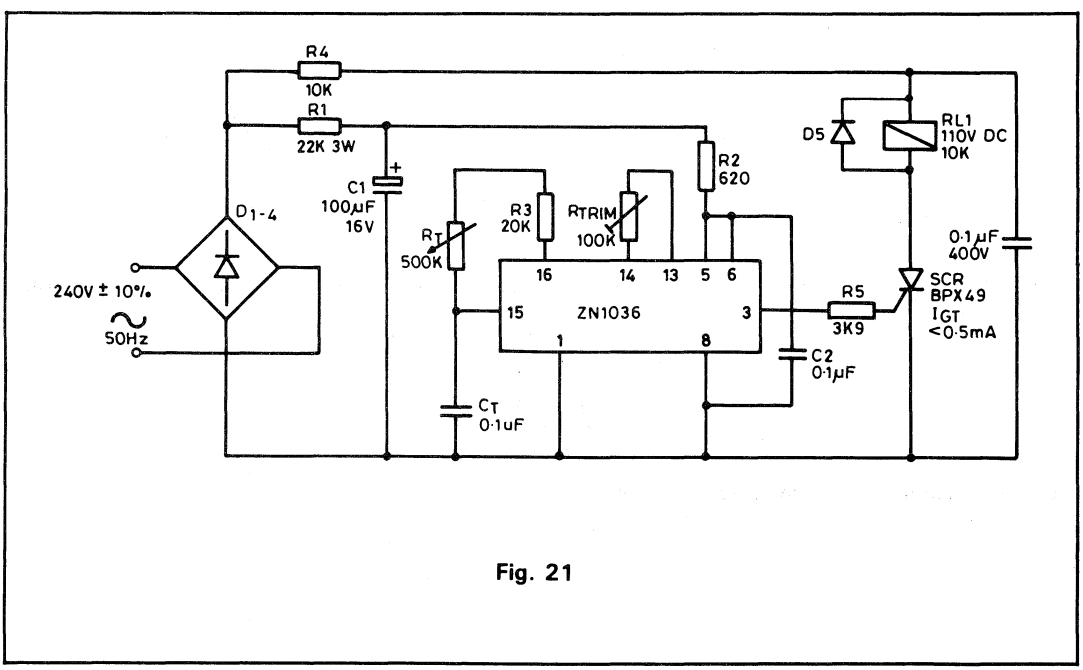


Fig. 21

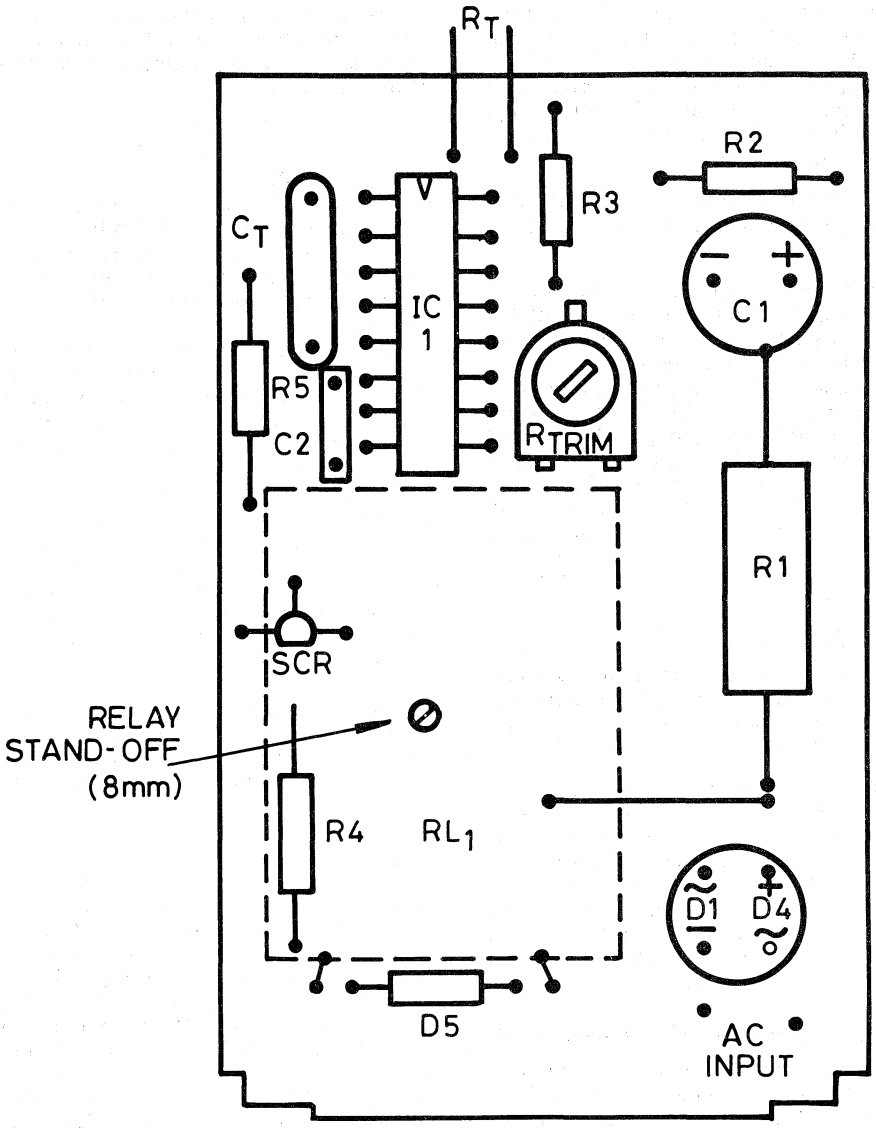

RT
R2
R3
CT
IC
1
C1
R5
C2
RTRIM
R1
SCR
RELAY
STAND-OFF
(8mm)
R4
RL1
D1
D4
D5
AC
INPUT

Fig. 22

Note 4.1 Mains borne interference

If the supply is reduced below (typically) 3.5V at any time, even for less than a microsecond then the logic and counter section of the ZN1036 will be reset and restoration of the normal supply may result in the initiation of a new timing period regardless of the initiation state. The effects of pulses on the supply are described in operating note 2.1.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig. 21 which rectifies the spikes as well as the a.c. supply, or a half bridge where an a.c. load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as d.c. regulation. The circuit of Fig. 21 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5 volt supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference.

If a transformer is used to isolate the timer from the mains then the voltage drop can be devided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V d.c. is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

Note 4.2 Electromagnetically induced noise

The ZN1036 oscillator frequency is determined by the time taken to change C_T via R_T from about 1.6 to 2.2 volts on pin 15. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1036 timer is made up of 511, 1023, 2047, or 4095 RC charging times then a large number of interference pulses in a timing period would be required to cause such a timing error. Where such interference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen pin 15 from eletro-magnetically induced noise. Since the oscillator is required to operate for example in one of its modes at

$$\frac{4095}{20 \times 10^{-3}} \text{ Hz},$$

i.e. 200kHz, pin 15 is sensitive to radiated high frequency interference. Mains borne pulses can be equally troublesome if steps are not taken to isolate pin 15 from such interference. The method used in the design example of Fig. 22 is effective against both EMI and Mains Borne noise. A ground plane is produced by leaving a large area of copper on the component side of a double sided PCB with clearance holes for the component connections. The ground pin (8) is connected to the earth plane and the earthy side of components such as C_T and the decoupling capacitors are also connected directly to the ground plane. In this way the connections have a low impedance to pin 8 and the possibility of coupling interference pulses from the load or decoupling components into the oscillator circuit via common earth leads is reduced considerably. At the same time the printed circuit connections are screened from EMI.

An external screen such as a metal case can be effective against radiated interference but it does not have the advantage of an earth plane with regard to the reduction of common earth lead interference.

Any leads connected to pin 15 are susceptable to interference pick-up and should be screened. A remote variable timing resistor can be connected to the PCB either by twin screened lead with the screen to ground or single screened with the screen connected to pin 16. It will be noticed that the fixed part of the timing resistance is connected very close to pin 15 to help decouple the connecting leads to the variable resistor.

When the ZN1036 oscillator frequency is near to that of the mains supply, or to low harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period.

SECTION 5 TIMER CALIBRATION

5.1 Direct measurement

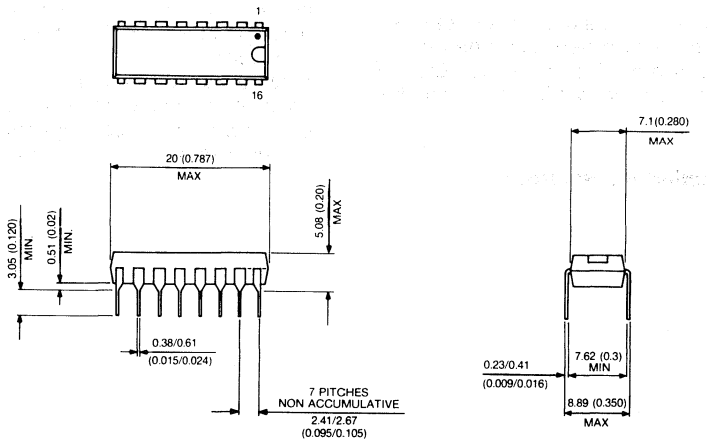
Timer circuits may be calibrated directly by measuring the time period between changes of state on the output pins 3 or 4. Accuracies of better than 0.2% can be achieved using this method.

5.2 Oscillator period measurement

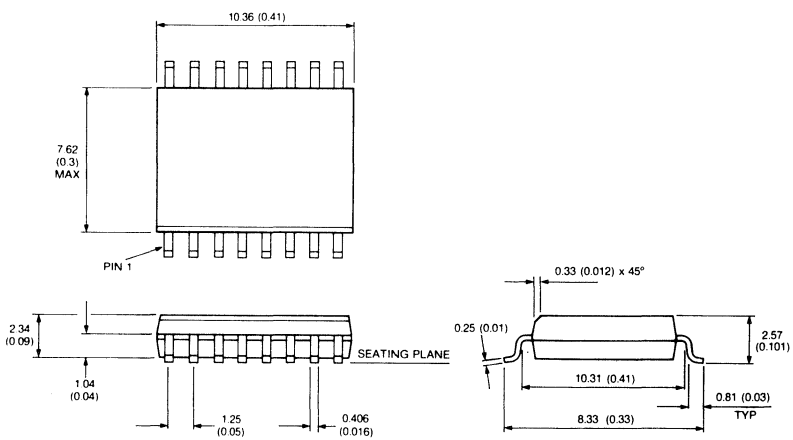
The measurement of oscillator period is a much quicker method of calibration and this is made possible on the ZN1036 by the inclusion of a low impedance output. This output is Pin 12 and an external pull up resistor of 5-10k is required. This enables the designer to calibrate the oscillator easily without affecting its operation and without the necessity for a high impedance probe.

PACKAGE DETAILS

Dimensions are in millimetres.



16-LEAD PLASTIC DIL - DP16



16-LEAD MINIATURE PLASTIC DIL (MP16 - WIDE BODY)

Plessey Semiconductors Locations

Main offices

HEADQUARTERS **Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext. 2198.

NORTH AMERICA **Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

International marketing centres

BENELUX **Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.

FRANCE **Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.

ITALY **Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.

UNITED KINGDOM (SOUTH) **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666 Ext.250.

UNITED KINGDOM (NORTH) **Plessey Semiconductors Ltd.,** Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.

WEST GERMANY, AUSTRIA and SWITZERLAND **Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.

SOUTH EAST ASIA **Plessey Company plc.,** Room 2204-7 Harbour Centre, 25 Harbour Road, Wanchai, Hong Kong. Tel: 58332111 Tx: 74754 Fax: 58339090.

World-wide agents

AUSTRALIA and NEW ZEALAND **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.

EASTERN EUROPE **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. U.K. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666.

GREECE **Mammeas,** Representations & Exportations, P.O.Box 181, Piraeus. Tel: 4172597 Tx: 213835 LHGR.

INDIA **Semiconductors Ltd.,** 71 Mittal Chambers, Nariman Point, Bombay 400 021. Tel: 2874518 Tx: 11 2781 ADOR IN.
Semiconductors Ltd., Unity Buildings, J.C. Road, Bangalore 560-001. Tel: 52072 & 578739.
Semiconductors Ltd., 513, Ashoka Estate, 24, Barakhamba Road, New Delhi — 110001. Tel: 44879 Tx: 31 3369.
Khandelwal Herrmann Electronics Limited, B-207, Neelam Centre, Worli, Bombay-400 025. Tel: 4947476.

JAPAN **Cornes & Company Ltd.,** Maruzen Building, 2 Chome Nihonbachi, Chuo-Ku, C.P.O.Box 158, Tokyo 100-91. Tel: 010 81 3 272 5771 Tx: 24874 Fax: 271-1479.
Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 532 1012 Tx: 525-4496 Fax: 541-8850.
Microtek Inc., Itoh Bldg., 7-9-17 Nishishinjuku, Shinjuku-ku, Tokyo 160. Tel: 03-371-1811 Tx: J27466 Fax: 03-369-5623.

HONG KONG **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kok Street, Tsuen Wan, N.T., Hong Kong. Tel: 0-444241-6 Tx: 36590 Fax: 499-3065.

KOREA **Young O Ind Co. Ltd.,** Yeoevido, P.O.Box 149, Seoul. Tel: 782 1707 Tx: K25701. Fax: 784 6786.
KML Corporation, 3rd Floor, Banpo Hall Building, 604-1 Banpo Dong, Kangnam-Ku, P.O.Box 19, Seoul. Tel: (02) 533-9281/2 Tx: KMLCORP K25981 Fax: (02) 533 1986.

MALAYSIA **Plessey Malaysia,** 1602 Pernas International Bldg, Jalan Sultan Ismail, Kuala Lumpur 50250. Tel: (03) 2611477 Tlx: 30918 PLESCOMA Direct Fax: (03) 2613385.

SCANDINAVIA

Denmark **Scansupply,** Nannasgade 18, DK-2200 Copenhagen N, Tel: 45 1 83 50 90 Tx: 19037 Fax: 45 1 83 25 40.

Finland **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 90 55 00 02 Tx: 122214 Fax: 055 1117.

Norway **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, Oslo 5. Tel: 02 64 11 50 Tx: 71963 Fax: 02 643443.

Sweden **Swedesupply AB,** PO Box 1028, 171 21 Solna. Tel: 08/735 81 30 Tx: 13435 Fax: 08/839033.

SINGAPORE **Plessey S.E. Asia Pte Ltd.,** 400 Orchard Road, No. 21-07 Orchard Towers, Singapore 0923. Tel: 7325000 Tx: RS22013 Direct Fax: 7329036.

SOUTH AFRICA **Plessey South Africa Ltd.,** 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793, Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SPAIN **JR Trading,** Apartado de Correos 8432, Madrid 8 Tel: 248 12 18/248 38 82 Tx: 42701. Fax: 241 4460.

TAIWAN **Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan, Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.

TURKEY **The Plessey Company plc.,** Koroglu Caddesi 5/4, Gaziosmanpasa, Ankara. Tel: 010 90 41 367352 Fax: 46526.

World-wide distributors

AUSTRALIA
Plessey Semiconductors Australia Pty Ltd., P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney (02) 720133 Tx: AA20384 Direct Fax: (02) 7260669.

AUSTRIA
DAHMS Elektronik Ges. mbH, Wiener Str. 287, A-8051 Graz. Tel: 0316/64030 Tx: 31099. Fax: 0316/6403029.
Othmar Lackner, Landstrasser Hauptstr. 37, A-1030 Wien. Tel: 0222 75 26 18-0 Tx: 111198. Fax: 0222/7526185.

BELGIUM
Master Chips, 4 St. Lazarus Laan, 1030 Brussels. Tel: 02 219 58 62 Tx: 62500. Fax: 02 217 92 01.

FRANCE
Mateleco:
Ile de France, 66, Avenue Augustin Dumont, 92240 Malakoff. Tel: (1) 46 57 70 55 Tx: 203436F.
Rhone-Alpes, 2 Rue Emile Zola, 38130 Echirolles. Tel: 76 40 38 33 Tx: 980837F.
ICC:
Bordeaux, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539F. Fax: 61 48 11 25.
Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalieres. Tel: 73 36 71 41 Tx: 990928F.
Marseille, Z.A. Artizanord II, 13015 Marseille. Tel: 91 03 12 12 Tx: 441313F.
Toulouse, 78 Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10 Tx: 520897F.
CGE Composants S.A.:
Ile de France, 32 Rue Grange Dame Rose, 92360 Meudon la Foret. Tel: (1) 46 30 24 45 Tx: 632253F Fax: 46 30 0081.
Aquitaine, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40 Tx: 571224F.
Bretagne, 9 Rue du General Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311F.
Centre/Pays-de-Loire, Allee de la Detente, 86360 Chaseneuil du Poitou. Tel: 49 52 88 88 Tx: 791525F.
Est, 27 Rue Kleber, 68000 Colmar. Tel: 89 41 15 43 Tx: 870569F.
Midi-Pyrenees, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38 Tx: 530957F.
Nord, 2 Rue de la Creativite, 59650 Villeneuve d'Ascq. Tel: 20 67 04 04 Tx: 136887F.
Provence/Cote d'Azur, Avenue Donadei, bat.B, 06700 St. Laurent du Var. Tel: 93 07 77 67 Tx: 461481F.
Rhone-Alpes, 101 Rue Dedieu, 69100 Villeurbanne. Tel: 78 68 32 29 Tx: 305301F.
ATAC-Diffusion SA, 2 Rue-Lecointre, 7 Ave de l'Europe, 92310 Sevres. Tel: 14 507 11 11 Tx: 203047 Fax: (1) 45341042.

ITALY
Eurelettronica SpA, Via E Fermi 8, 20090 Assago (Milan). Tel: 02-4880022 Tx: 350037. Fax: 488 0275.
Eurelettronica, Via Bertoloni 27, Rome. Tel: 875394 Tx: 610358.
Alta S.R.L., Via Matteo Di Giovanni 6, 50143 Florence. Tel: 055717402 Tx: 571246. Fax: 055/705658.
Adelsi Spa, Via Novara 570, 20153 Milan. Tel: 02 3580641 Tx: 332423 Adelsy I Fax: 02/3011988.
ESCO Italiana Spa., Via Modena 1, 20099 Sest S Giovanni. Tel: 02 24 09 241-251 Tx: 322383. Fax: 02/2409255.
Fanton S.R.L., Bologna, Milano, Firenze, Roma, Padora, Torino. Tel: (02) 3287312 Fax: 051/732216.

NETHERLANDS
Heynen B.V., Postbus 10, 6590 AA Gennep. Tel: 8851-96111 Tx: 37282 Fax: 08851 96220.
Tekelek Airtronic BV., Postbus 63-2700 AB, Zoetermeer. Tel: 079 31010 Tx: 33332. Fax: 079 417504.

SOUTH AFRICA
Plessey South Africa Ltd., 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793 Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SWITZERLAND
Aumann & Co. AG, Forrlibuckstrasse 150, CH-8037 Zurich. Tel: 01/443300 Tx: 822966. Fax: 01/44 5023.
Elbatex AG., Hardstr. 72, 5430 Wettingen. Tel: 056 27 51 11 Tx: 58068 Fax: 056/271924.

TAIWAN
Artistex International Inc., B2, 11th Floor, 126, Nanking East Road, Section 4, Taipai, Taiwan, Republic of China. Tel: (02) 7526330 Tx: 27113 ARTISTEX Fax: (8862) 721 5446.

UNITED KINGDOM
Celdis Ltd.,37-39 Loverock Road, Reading, Berks RG3 1ED. Tel: 0734 585171 Tx: 848370 Fax: 0734 509933.
Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU. Tel: 0532 636311 Tx: 55147 Fax: 0532 633404.
Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878/787848 Tx: 847571 Fax: 0734 776095.
Gothic Crellon Ltd., P.O.Box 301, Trafalgar House, 28 Paradise Circus, Queensway, Birmingham B1 2BL. Tel: 021 6436365 Tx: 338731.
RR Electronics Ltd., St. Martins Way, Cambridge Road, Bedford MK42 0LF. Tel: 0234 47188/270777 Tx: 826251 Fax: 0234 210674.
Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street, Yiewsley, West Drayton, Middlesex UB7 7XB. Tel: 0895 445522 Tx: 21958 Fax: 0895 422044.

STC Electronic Services, Edinburgh Way, Harlow, Essex CM20 2DF.Tel: 0279 626777 Tx: 818801. Fax: 0279 441687.
Unitel Ltd., Unitel House, Fishers Green Road, Stevenage, Herts. Tel: 0438 312393 Tx: 825637. Fax: 0438 318711.

UK EXPORT (to countries other than those listed)
Extram (U.K.) Ltd., 1A Albert St., Slough, Berks. SL1 2BH. Tel: 0753 824311 Tx: 848441 EXTRAM G Fax: 0753 820250.

WEST GERMANY
Altron GmbH & Co. KG, Gaussstr. 10, 3160 Lehrte. Tel: 051 32 5 30 24 Tx: 922383 Fax: 05132/57776.
API Elektronik Vertriebs GmbH, Augustinerring 27, D-8062 Markt Indersdorf. Tel: 08136/7092 Tx: 5270505 Fax: 08136/7398.
AS Electronic Vertriebs-GmbH, Elisabethenstrasse 35, 6380 Bad Homburg. Tel: 06172/2 90 28-29 Tx: 410868.
Astronic GmbH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187 Fax: 089 300 6001.
Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708. Fax: 07159/5119.
Weisbauer Elektronik GmbH, Heiliger Weg 1, 4600 Dortmund 1. Tel: 0231 57 95 47 Tx: 822538 Fax: 0231/577514.

North American representatives

NATIONAL SALES — Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066. United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

EASTERN REGION — 1767-42 Veterans Memorial Hwy., Central Islip, NY 11722. Tel: (516) 582-8070 Tlx: 705922 Fax: 516-582-8344.

NEW ENGLAND REGION — 132 Central St., 216 Foxboro, MA 02035. Tel: (617) 543-3855 Tlx: 316805 Fax: 617-543-2994.

WESTERN REGION — 4633 Old Ironsides Dr. 250, Santa Clara, CA 95054. Tel: (408) 986-8911 Tlx: 62217370 Fax: 408-970-0263.

SOUTHEAST REGION — 9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930 Tlx: 510-600-3635 Fax: 214-680-9753.

NORTH CENTRAL REGION — 1919 South Highland 120C, Lombard, IL 60148. Tel: (312) 953-1484 Tlx: 705186 Fax: 312-953-0633.

FLORIDA & DIXIE REGION — 541 S.Orlando Ave., Suite 310, Maitland, FL 32751. Tel: (305) 539-0080 Fax: 304-539-0055.

SOUTHWEST REGION — 9 Parker, Irvine, CA 92718. Tel: (714) 472-2530 Tlx: 989096 Fax: 714-458-7084.

DISTRIBUTION SALES — 9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Tlx: (910) 595-1930 Fax: (714) 770-0627.

CANADA — 207 Place Frontenac, Quebec, H9R-4Z7. Tel: (514) 697-0095/96 Fax: 514-697-0681.

North American sales offices

ALABAMA — **DHR Marketing, Inc.,** 904 Bob Wallace Avenue, Suite 222, Huntsville, AL 35801. Tel: (205) 533-5165 Fax: (205) 533-1312.

ARIZONA — **Reptronix/Chaparral,** 4625 South Lakeshore Dr., Tempe, AZ 85282-7127. Tel: (602) 345-4580 Fax: (602) 839-3841.

CALIFORNIA — **Cerco,** 5230 Carrol Canyon Rd. 214, San Diego, CA 92121. Tel: (619) 450-1754 Fax: 619-450-3681.
Pinnacle Sales Corp., 275 Saratoga Ave., Suite 200, Santa Clara, CA 95050. Tel: (408) 249-7400 Fax: 408-249-5129.
Select Electronics, 2109 Brookfield Drive, Thousand Oaks, CA91362.
Straube Associates, 2551 Casey Avenue, Mountain View, CA 94043. Tel: (415) 969-6060 Fax: (415) 964-6526.
Select Electronics, 14730 Beach Blvd-Bldg F, Suite 106, La Mirada, CA 90638. Tel: (714) 739-8891 Twx: 910-596-2818 Fax: 714-739-1604.

COLORADO — **MRC,** 2579 W. Main St. Littleton, CO 80120. Tel: (303) 794-4684 Fax: (303) 794-4644.

CONNECTICUT — **NRG Ltd.,** 63 Duka Avenue, Fairfield, CT 06430. Tel: (203) 384-1112 Fax: (203) 335-2127.

FLORIDA — **Lawrence Associates,** 1131 South U.S.19 Palm Barbor, FL 34684. Tel: (813) 787-2773 Fax: (813) 787-2654.
Lawrence Associates, 380 Lowndes Square, Casselberry, FL 32707. Tel: (305) 339-3855 Fax: (305) 767-0973.
Lawrence Associates, 5021 N. Dixie Highway, Boca Raton, FL 33431. Tel: (305) 368-7373 Fax: 305-394-5442.

GEORGIA — **DHR Marketing, Inc.,** 3100 Breckenridge Blvd. Suite 145, Duluth, GA 30136. Tel: (404) 564-0529 Fax: (404) 564-1127.

IDAHO — **Crown Electronic Sales, Inc.,** 601 W. Hays, Suite 20, Boise, Idaho 83702. Tel: (208) 344-9588 Fax: (208) 344-9550.

INDIANA	**Corrao Marsh, Inc.,** 6211 Stoney Creek Drive, Fort Wayne, IN 46825. Tel: (219) 482-2725 Fax: 219-484-7491.
	Corrao Marsh, Inc., 3117 West U.S. 40, Greenfield, IN 46140. Tel: (317) 462-4446. Fax: (317) 462-6568.
ILLINOIS	**Micro Sales, Inc.,** 54 West Seegars Road, Arlington Heights, IL 60006. Tel: (312) 956-1000 Twx: 510-600-0756 Fax: 312-956-0189.
IOWA	**Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666 Fax: 319-377-2273.
KANSAS	**Lorenz Sales, Inc.,** 8115 West 63rd St., Suite 1, Merriam, KS66202. Tel: (913) 384-6556.
MARYLAND	**Walker-Houck,** 10706 Reisters Town Rd., Suite D, Owings Mills, MA 21117. Tel: (301) 356-9500 Fax: 301-356-9503.
MASSACHUSETTS	**Stone Components,** 2 Pierce Street, Framingham, MA 01701. Tel: (617) 875-3266 Twx: 310-374-6662 Fax: 617-875-0537.
MICHIGAN	**R.P. Urban & Associates,** 2335 Burton Street SE, P.O. Box 7386, Grand Rapids, MI49510. Tel: (616) 245-0511 Fax: (616) 245-4083.
	R.P. Urban & Associates, 24634 Five Mile Road, Detroit, MI48239. Tel: (313) 535-2355 Fax: (313) 7109.
MINNESOTA	**Electro Mark Inc.,** Valley Oaks Business Cntr. 7167 Shady Oak Rd., Eden Prairie, MN 55344. Tel: (612) 944-5850 Fax: (612) 944-5855.
MISSOURI	**Lorenz Sales, Inc.,** Del Crest Plaza Bldg. Suite 208, 8420 Delmar Blvd., University City, MO 63124. Tel: (314) 997-4558 Fax: 319-337-2273.
NEBRASKA	**Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660.
NEW JERSEY	**Metz Benham Associates, Inc., (MBA),** Terrace Level, Suite II, 1982 Greentree Road, Cherry Hill, NJ 08003. Tel: (609) 424-0404 Fax: (609) 751-2160.
	Metro Logic, 280 Midland Ave., Bldg N-1, Saddle Brook, NJ 07662. Tel: (201) 797-8844 Fax: 201-797-8418.
NEW MEXICO	**Reptronix/Chaparral,** 237 C Eubank Blvd., N.E., Albuquerque, NM 87123. Tel: (505) 292-1718 Fax: (505) 299-1611.
NEW YORK	**Micro-Tech,** 1350 Buffalo Road, Rochester, NY 14624. Tel: (716) 328-3000 Fax: (716) 328-3003.
	Micro-Tech, 401 South Main Street, North Syracuse, NY 13212. Tel: (315) 458-5254 Fax: (315) 458-5919.
	Micro-Tech, 10 Guyton Street, Kingston, NY 12401. Tel: (914) 338-7588.
NORTH CAROLINA	**DHR Marketing, Inc.,** 4016 Barrett Drive, Suite 201 (27609) P.O. Box 19703, Raleigh, NC 27609. Tel: (919) 781-1961
SOUTH CAROLINA	**DHR Marketing, Inc.,** 37 Villa Road, Suite 409, Greenville, SC 29615. Tel: (803) 271-8712 Fax: (803) 271-8712.
OHIO	**Scott Electronics, Inc.,** 3131 S. Dixie Dr., Suite 200, Dayton, OH 45439. Tel: (513) 294-0539 Fax: (513) 294-4769.
	Scott Electronics, Inc., 360 Alpha Park, Cleveland, OH 44143. Tel: (216) 473-5050 Fax: (216) 473 5055.
	Scott Electronics, Inc., 6515 East Livingston Avenue, Reynoldsburg, OH 43068 Tel: (614) 1281 Fax: (614) 863-1485.
	Scott Electronics, Inc., 10901 Reed Hartman Hwy., Suite 301, Cincinnati, OH 45242. Tel: (513) 791-2513 Fax: (513) 791-8059.
OREGON	**Core II, P.O. Box 5459, Beaverton, OR 96006-0459.** Shipping Address only: 21785 S.W. T.V. Hwy, Unit Q, Beaverton, OR 97006. Tel: (503) 641-0877 Fax: (503) 591-8383.
	Crown Electronic Sales, Inc., 17020 S.W. Upper Boones Ferry Rd., Suite 202, Portland, OR 97223. Tel: (503) 620-8320 Fax: 503-639-4023.
TENNESSEE	**DHR Marketing, Inc.,** 417 Welchwood, Suite 102, Nashville, TN 37211.Tel: (615) 331-2745.
TEXAS	**Oeler & Menelaides, Inc.,** 8340 Meadow Rd., Suite 24, Dallas, TX 75231. Tel: (214) 361-8876 Fax: (214) 692-0235.
	Oeler & Menelaides, Inc., 12777 Jones Rd., Suite 175-18, Houston, TX 77070. Tel: (713) 894-5021.
	Oeler & Menelaides, Inc., 8705 Shoal Creek Rd., Suite 218, Austin, TX 78758. Tel: (512) 453-0275 Fax: (512) 453-0088.
WASHINGTON	**Core II,** 2535 152nd N.E. Suite A, Redmond, WA 98052. Tel: (206) 746-1799 (Home).
	Crown Electronic Sales, Inc., 14400 Bel-Red Rd., 108, Bellevue, WA 98007. Tel: (206) 643-8100 Fax: 206-747-6861.
WISCONSIN	**Micro Sales, Inc.,** N8 W12920 Leon Road, Suite 115, Menomonee Falls, WI 53051. Tel: (414) 251-0151.
CANADA EASTERN	**Gidden-Morton Assoc.Inc.,**7050 Bramalea Road, Suite 27A, Mississauga, Ontario L5S 1T1. Tel: (416) 671-8111 Fax: (416) 671-2422.
	Gidden-Morton Assoc.Inc.,3860 Cote-Vertu, Suite 221, St. Larent, Quebec H4R 1N4. Tel: (514) 335-9572 Fax: 514-335-9573.
	Gidden-Morton Assoc.Inc.,301 Moodie Drive, Suite 101, Nepean, Ontario K2H 9C4. Tel: (613) 726-0844 Fax: 613-726-0953.
CANADA WESTERN	**Dynasty Components, Inc.,** 12618 55A Avenue, Surrey, British Columbia V3W 1C3. Tel: (604) 597-0068 Fax: (604) 597-0043.

American design centres

ARIZONA **CaDel,** 715 N. Constitution Drive, Dueson, AZ 85748. Tel: (602) 296-8591.

CALIFORNIA **Analog Solutions,** 532 Fourth Street, Encinitas, CA 92024. Tel: (619) 944-1657.
Silicon Development Corp., 16162 Beach Boulevard, Suite 304, Huntington Beach, CA 92647. Tel: (714) 847-1992.

CANADA **Ontario Centre for Microelectronics,** 1150 Morrison Drive, Suite 400, Ottawa, K2H 9B8. Tel: (613) 596-6690.
Alberta Microelectronics Center, Suite 200, 1620-29 St., N.W., Calgary, Alberta T2N 4L7. Tel: (403) 289-2043.

COLORADO **Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.

FLORIDA **Silicon Beach Enterprises, Inc.,** 700 U.S. Highway One, Suite C, North Palm Beach, FL 33408. Tel: (305) 844-7805.

ILLINOIS **Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Road, Arlington Heights, IL 60005. Tel: (312) 956-0710.

MARYLAND **MicroCom Design, Inc.,** 9696 Deere Co. Road, Timonium, MD 21093.Tel: (301) 561-4811.

MASSACHUSETTS **Custom Silicon, Inc.,** 600 Suffolk Road, Lowell, MA 01854. Tel: (617) 454-4600.

North American distributors

ALABAMA **Pioneer/Technologies,** 4825 University Square, Huntsville, AL 35805. Tel: (205) 837-9300 Twx: 810-726-2197.
Hammond, 4411 B Evangel Circle, Huntsville, AL 35816. Tel: (205) 830-4764. Fax: (205) 830-4287.

ARIZONA **Insight Electronics,** 1525 W. University Dr., Suite 105, Tempe, AZ 85282. Tel: (602) 829-1800 Twx: 510-601-1618 Fax: (602) 967-2658.
Wyle-Phoenix, 17855 No. Black Canyon Hwy., Phoenix, AZ 85023. Tel: (602) 866-2888 Fax: 602-866-6937.

CALIFORNIA **Cypress Electronics (Corp.),** 2175 Martin Ave., Santa Clara, CA 95050. Tel: (408) 980 2500 Fax: (408) 986-9584.
Cypress Electronics, 6230 Descanso Ave., Buena Park, CA 90620. Tel: (714) 521-5230 Tlx: 5215716 Fax: (714) 521-5716.
Insight Electronics (Corp.), 6885 Flanders Dr., Unit G, San Diego, CA 92121. Tel: (619) 587-0471 Twx: 183035 Fax: (619) 587-1380.
Insight Electronics, 28035 Dorothy Dr., Suite 220, Agoura CA 91301. Tel: (818) 707-2100 Fax: (818) 707-0321.
Insight Electronics, 3505 Cadillac Ave., Unit E-1, Costa Mesa CA 92626. Tel: (714) 556-6890 Twx: 62354990 Fax: (714) 556-6897.
Pacesetter Electronics, 5417 E. La Palma Avenue, Anaheim, CA 92807. Tel: (714) 779-5855.
Wyle-Santa Clara, 3000 Bowers Av., Santa Clara, CA 95051. Tel: (408) 727-2500 Twx: 910-338-0296 Fax: 408-727-5896.
Wyle-Sacramento, 11151 Sun Center Drive, Rancho Cordova, CA 95670. Tel: (916) 638-5282 Fax: 916-638-1491.
Wyle-Irvine, 17872 Cowan Ave., Irvine, CA. Tel: (714) 863-9953 Twx: 3719599 Fax: (714) 863-0473.
Wyle-L.A./San Fernando, 26677 West Agoura Rd., Calabasas, CA 91302. Tel: (818) 880-9000 Twx: 3103720232 Fax: 818-880-5510.
Wyle-San Diego, 9525 Chesapeake Dr., San Diego, CA 92123. Tel: (619) 565-9171 Fax: 619-565-0512.

NORTH CAROLINA **Hammond,** 2923 Pacific Ave., Greensboro, NC 27406. Tel: (919) 275-6391 Tlx: 62894645 Fax: (919) 275-6391.
Pioneer/Technologies, 9801A South Pine Blvd., Charlotte, NC 28210. Tel: (704) 527-8188 Twx: 810-621-0366.

COLORADO **Cypress Electronics,** 12441 West 49th Ave., Wheatridge, CO 80033. Tel: (303) 431-2622 Fax: (303) 431-7191.
Wyle-Denver, 451 East 124th St., Thornton, CO 80241. Tel: (303) 457-9953 Twx: 9109360770 Fax: 303-457-4831.

CONNECTICUT **Jaco Electronics,** 384 Pratt Street, Meriden, CT 06450. Tel: (203) 235-1422.
Pioneer/Standard, 112 Main Street, Norwalk, CT 06851. Tel: (203) 853-1515 Twx: 710 468 3373.

FLORIDA **All American,** 16251 NW 54th Avenue, Miami, FL33014. Tel: (305) 621-3282.
Hammond (Corp.), 6600 N.W. 21st Ave., Ft. Lauderdale, FL 33309. Tel: (305) 973-7103 Twx: (510) 956-9401.
Hammond, 1230 West Central Blvd., Orlando, FL 32802. Tel: (305) 849-6060 Twx: 810-850-4121 Fax: (305) 648-8584.
Pioneer/Technologies, 674 South Military Trail, Deerfield Beach, FL 33442. Tel: (305) 428-8877 Twx: 510-955-9653.
Pioneer/Technologies, 337 South Northlake Blvd., Suite 1000, Altamonte Springs, FL 32701. Tel: (305) 834-9090 Twx: 810-853-0284.

GEORGIA	**Hammond,** 5860 Oakbrook Pkwy, Suite 160, Norcross, GA 30093. Tel: (404) 449-1996 Fax: (404) 242-9834.
	Pioneer/Technologies, 3100 F Northwoods Pl., Norcross, GA 30071. Tel: (404) 448-1711 Twx: 810-766-4515.
INDIANA	**Pioneer/Standard,** 6408 Castleplace Dr., Indianapolis, IN 46250. Tel: (317) 849-7300 Twx: 810-260-1794.
ILLINOIS	**Advent Electronics,** Rosamont, IL 60018. Tel: (312) 297-6200 Twx: 910 233 2477.
	Pioneer/Standard, 2171 Executive Drive, Addison, ILL 60101. Tel: (312) 495-9680.
KANSAS	**Pioneer,** 10551 Lackman Rd., Lenexa, KS 66215. Tel: (913) 492-0500 Twx: 510-601-6411.
MASSACHUSETTS	**Emtel Electronics,** 375 Vanderbilt Ave., Norwood, MA 02062. Tel: (617) 769-9500 Fax: (617) 769-8329.
	Jaco Electronics, 222 Andover Street, Wilmington, MA 01877. Tel: (617) 273-1860.
	Pioneer/Standard, 44 Hartwell Avenue, Lexington, MA 02173. Tel: (617) 861-9200 Twx: 710-326-6617.
	Textrel Semi (Die only), 56 Middlesex Turnpike, Burlington, MA 01303. Tel: (617) 270-9246.
MARYLAND	**Jaco Electronics,** Rivers Center, 10270 Old Columbia Road, Columbia, MD 21046 Tel: (301) 995-6620.
	Pioneer/Tech. Group. Inc., 9100 Gaither Rd., Gaithersburg, MD 20877. Tel: (301) 921-0660 Twx: 710-828-0545 Fax: (301) 921-4255.
MICHIGAN	**Pioneer/Standard,** 13485 Stamford, Livonia, MI 48150. Tel: (313) 525-1800 Twx: 810-242-3271.
	Pioneer, 4505 Broadmoore Ave., S.E., Grand Rapids, MI 49508. Tel: (616) 698-1800 Twx: 510-600-8456.
MINNEAPOLIS	**Cypress Electronics,** 7650 Executive Drive, Eden Prairie, MN 55334. Tel: (612) 934-2104 Fax: (612) 934 2057.
	Industrial Components, Inc., Minneapolis, MN 55435. Tel: (612) 831-2666 Twx: 910 576 3153.
	Pioneer/Standard, 10203 Bren Road East, Minnetonka, MN 55343. Tel: (612) 944-3355 Twx: 910-576-2738.
NEW JERSEY	**Jaco Electronics,** 555 Preakness Road, Tontoa, NJ 07512. Tel: (201) 942-4000.
	Pioneer/Standard, 45 Rte. 46 Pinebrook, NJ 07058. Tel: (201) 575-3510 Twx: 710-734-4382.
	General Components, Inc., 245 D Clifton Ave., W. Berlin, NJ 08091. Tel: (609) 768-6767 Twx: 920-333-3057.
NEW YORK	**Add Electronics,** 7 Adler Drive, E. Syracuse, NY 13057. Tel: (315) 437-1835.
	Jaco Electronics, Hauppauge, NY 11787. Tel: (516) 273-5500 Twx: 510-227-6232 Fax: (516) 273-5799.
	Mast, 95 Oser Ave., Hauppauge, NJ 11788. Tel: (516) 273-4422 Twx: 4974384.
	Pioneer/Standard, 68 Corporate Drive, Binghamton, NY 13904. Tel: (607) 722-9300 Twx: 510-252-0893.
	Pioneer/Standard, 60 Crossways Park West, Woodbury, NY 11797. Tel: (516) 921-8700 Twx: 510-221-2184 Fax: (516) 921-2143.
	Pioneer/Standard, 840 Fairport Park, Fairport Park, NY 14450. Tel: (716) 381-7070 Twx: 510-253-7001.
OHIO	**Pioneer/Standard,** 4800 East 131st St., Cleveland, OH 44105. Tel: (216) 587-3600 Twx: 810-421-0011 Fax: (216) 587-3906.
	Pioneer, 4433 Interpoint Bl., Dayton, OH 45424. Tel: (513) 236-9900 Twx: 810 459 1622.
OREGON	**Cypress Electronics,** 15075 S.W. Coll Parkway, Suite D, Beaverton, OR 97006. Tel: (503) 641-2233 Fax: (503) 643-1237.
	Wyle-Portland, 5250 N.E. Elam Young Pkwy., Suite 600, Portland, OR 97123. Tel: (503) 640-6000 Fax: 503-640-5846.
PENNSYLVANIA	**Advacom Electronics,** 5620 West Road, McKean, PA 16426. Tel: (814) 476-7774.
	Pioneer/Technologies, 261 Gibraltar Rd., Horsham, PA 19044. Tel: (215) 674-4000 Twx: 510-665-6778.
	Pioneer/Standard, 259 Kappa Drive, Pittsburg, PA 15238. Tel: (412) 782-2300 Twx: 710-795-3122.
TEXAS	**Pioneer/Standard,** 9901 Burnet Road, Austin, TX 78758. Tel: (512) 835-4000 Twx: 910-874-1323.
	Pioneer/Standard, 13710 Omega Road, Dallas, TX 75244. Tel: (214) 386-7300 Twx: 910-860-5563 Fax: (214) 490-6419.
	Pioneer/Standard, 5853 Point West Drive, Houston, TX 77056. Tel: (713) 988-5555 Twx: 910-881-1606 Fax: (713) 988-1732.
	Wyle-Dallas, 1810 North Greenville Ave., Richardson, TX 75083. Tel: (214) 235-9953 Fax: 214-644-5064.
	Wyle-Houston, 11001 So. Hilcrest, Suite 100, Houston, TX 77099. Tel: (713) 879-9953 Fax: 713-879-6540.
	Wyle-Austin, 2120 F West Braker Lane, Austin, TX 78758. Tel: (512) 834-9957 Fax: 512-834-0981.
UTAH	**Wyle-Salt Lake City,** 1325 West 2200 South, Suite E, West Valley, Utah 84119. Tel: (801) 974-9953 Fax: 801-972-2524.
WASHINGTON	**Cypress Electronics,** 22125 17th Ave., S.E., Suite 114, Bothell, WA 98021. Tel: (206) 483-1144 Fax: (206) 485-1512.

	Wyle-Seattle, 15385 N.E. 90th Street, Redmond, WA 98052. Tel: (206) 881-1150 Twx: 3103724260 Fax: (206) 881-1567.
CANADA EASTERN	**Carsten Electronics,** 3791 Victoria Park Avenue, Scarborough, Ontario, M1K3K6. Tel: (416) 495-7705.
	Semad, 243 Place Frontenac, Pointe Claire, P.Q. N9R 4Z7. Tel: (514) 694-0860 Twx: 05821861 Fax: (514) 694-0965.
	Semad, 1827 Woodward Dr., Suite 303, Ottawa, Ontario K2C 0R3. Tel: (613) 727-8325 Twx: 0533943 Fax: (613) 727 9489.
CANADA WESTERN	**Semad,** 75 Glendeer Dr., SE., Suite 210, Calgary, Alberta T2H 2S8. Tel: (403) 252-5664 Twx: 03824775.
	Semad, 3700 Gilmore, Suite 210, Burnaby, BC V5G 4M1. Tel: (604) 438-2515 Twx: 04356625.
	Semad, 85 Spy Court, Markham, Ontario, L3R 4Z4. Tel: (416) 475-3922 Twx: 06966600. Fax: (416) 475 4158.

Primary semi-custom design centres

AUSTRALIA	**Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.
BENELUX	**Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.
FRANCE	**Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.
ITALY	**Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.
WEST GERMANY	**Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.
TAIWAN	**Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan. Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.
UNITED KINGDOM	**Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW. United Kingdom Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext: 2198.
	Plessey Semiconductors Ltd., Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.
UNITED STATES OF AMERICA	**Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576

Our world-wide distribution network is continually being updated; please check with your local Plessey Sales office for latest information.

Publication No. P.S.2008 October 1988

PWC 2049 10/88


PLESSEY
Plessey Semiconductors